

CPU, Glitchbus Interface, and Control

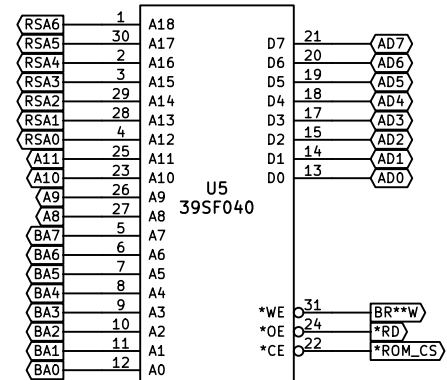
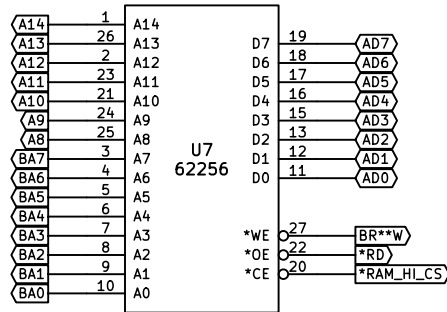
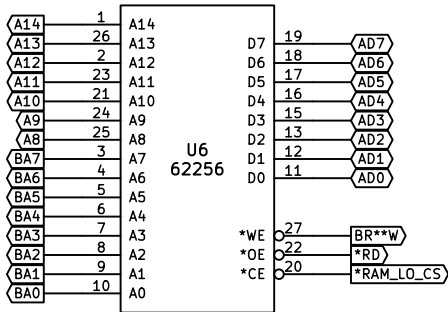
J. Chapman
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File: gw-8085sbc-4m.sch

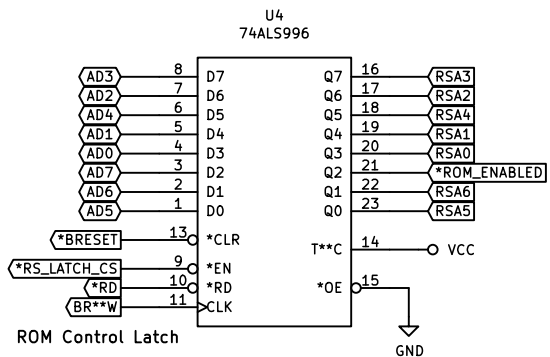
Title: 8085 SBC rev 4 Mini

Size: USLetter	Date: 2024-03-07
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Rev: PRODUCTION
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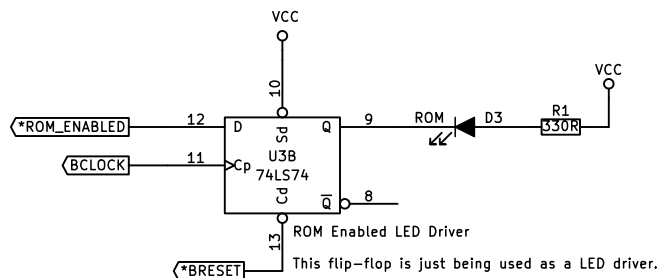
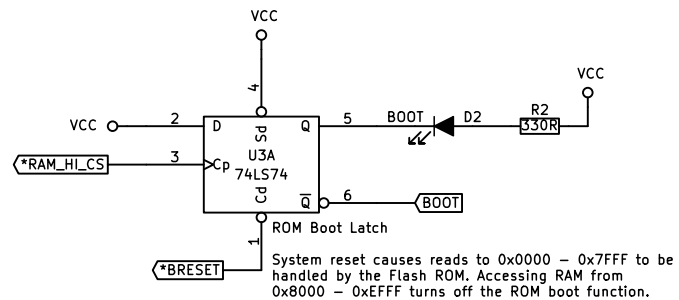


Memory Devices



ROM Control Latch

This latch controls which 4K segment of ROM is addressed. Cleared to 0 on *RESET, writable at IO_BASE + 2. Bits 0 - 6 set ROM page, bit 7 disables ROM when set to 1.



Memory Devices, ROM Segment Control, Boot Control

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Sheet: /Memory Devices/
File: memory.sch

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