DA JEN ELECTRONICS

System Central Interface SCI

SCI Specifications

3 independent parallel ports, each bit programmable input or latched output. Handshake signals for each port.

Serial port with RS-232, 20ma, 60ma current loops, speed selectable between 45 and 9600 baud.

High-speed biphase cassette interface with selectable speeds from 800 to 100,000 baud. Can also be used as a signal generator to test audio equipment.

Two on-board relays control two recorders. Three status lines for external recorder control.

Reset-jump: on reset, the CPU jumps to the SCI monitor.

2708 programmer.

256 bytes of RAM for stack and buffer space.

2k monitor in 2708's provides system control and I/O.

SCI requires the following S-100 bus signals:

+8 volts, +16 volts, -16 volts, circuit ground

$\overline{\text{PWR}}$, PDBIN, $\overline{\text{PHOLD}}$, $\overline{\text{PRESET}}$, PSYNC

SINP, SOUT

A0-A15, DI0-DI7, D00-D07

2 mhz clock

Power Requirements: (nominal)

+8 - 450 ma
+16- 85 ma
-16- 65 ma

Dimensions: 10.0 " wide x 5.1 " high (excluding edge connector)

SCI generates its own wait states, independent of the processor used, and can use 650ns 2708's.

SYSTEM CENTRAL INTERFACE

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A note of caution: This is an expensive interface. To protect your investment, and ensure a long operating life, exercise care in the construction of this board. Take your time, be certain of parts placement, don't force I.C.'s into their sockets, solder thoroughly, but sparingly, as a little solder goes a long way. Handle the I.C.'s carefully, making sure that the pins are straight before inserting them into their sockets. I.C. pins can break, and lead receptacles damaged, by careless insertion. Take the time to inspect and test the finished board before applying power. This avoids the smoke test.

Personal care: wear eye protection when cutting leads and soldering. This prevents foreign material from entering your eyes.

Use a metallic holder for the soldering iron. This prevents heat-damaged tables, possible fires, and carpet burns when soldering irons get loose. The soldering iron need only be 25 watts with a 1/8 inch spade tip. A welder is not necessary. An iron with a three-wire cord is preferable for electrical safety. An Ungar #135 is an excellent iron for p.c. work, and costs about $8.00. Rosin-core solder is supplied with the kit. If it's not enough, use 60/40 lead-tin rosin-core solder only. Acid-core solder will destroy the circuit and void the warranty.

All parts mount on the FRONT side, and solder on the BACK. Solder the parts after each step.

☑ Check the parts list and the parts layout. These should agree with the parts supplied. Contact us immediately if anything is missing, as shipping takes time.

☑ Locate the 7-pole DIP switch. Mount it in the upper left corner of the board. Mount it with the numbers toward the top of the board.

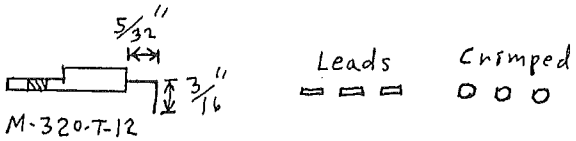
☑ Note the orientation of the I.C.'s: For vertical I.C.'s, pin 1 is to the upper left, and for horizontal I.C.'s, pin 1 is to the upper right.

☑ Install the three standard profile 24-pin sockets in pads 17,18, and 19. These are the sockets for the 2708's.

Note that I.C. pad 6 is the address jumper pad and does not have a socket.

☑ Install the remaining sockets.

☑ Install the four regulators and the two heat sinks. Line up the heat sinks over the areas marked on the p.c. board. Bend the leads of the regulators at right angles as shown on the parts list. The holes for the LM-320-T-12 were small on early production boards, and the leads of the regulator should be bent and cut approximately as shown, then crimp the leads slightly with pliers so they will fit the p.c. holes. Use 4-40 nuts and bolts to secure the regulators.



☑ Next, install the capacitors. Observe the polarity of the 16 tantalum capacitors: the + lead must line up with the + shown in the layout and marked on the p.c. board.

The - lead for the tantalum capacitor on the right-hand side of the board must be bent inward, to avoid hitting the guide rails of the card rack.

☑ Install the diodes, being careful to align the cathode bands with the markings on the p.c. board and shown in the layout drawing.

All resistors mount vertically: 

☑ Install the 1/2 watt resistors. These are about 50% larger than the 1/4 watt resistors. All are near IC-45.

☑ Install the remaining resistors.

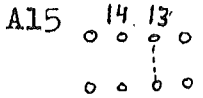
☑ There are two types of small-signal transistors used: 2N3904 and 2N3906. Be sure to place them at the correct locations, and oriented as shown in the layout. Spread the leads slightly to fit the hole patterns.

☑ The MJE-180 transistor in the upper right-hand corner of the board, has leads that must be crimped slightly to fit the mounting holes. Trim the leads, then crimp with pliers to fit.

☑ Insert the LED's, noting that the flat edge is the cathode. Check the parts list for details.

Jumper Options

☑ Strap the address jumpers for the board address you specified when ordering. If you didn't specify, D000 hex is the standard address in the firmware supplied by DAJEN.



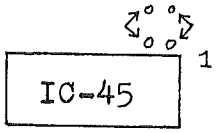
Address pad, D000 shown

ADDRESS	Jumper(s)	ADDRESS	Jumper(s)
8000 hex	A-12,13,14	C000 hex	A-12,13
9000	A-13,14	D000	A-13
A000	A-12,14	E000	A-12
B000	A-14	F000	None

Lower addresses (6000,7000) could be used, but are not recommended, as system RAM usually occupies the first 32 K of memory space, if not more.

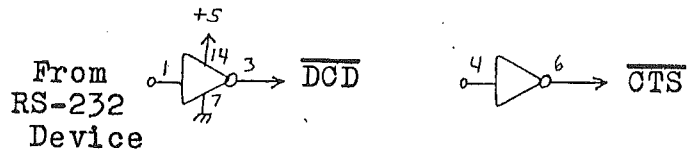
Note: I/O addresses use 16 consecutive ports, with the same byte as the board address. For a board address of D000, the I/O addresses are: D0,D1,D2,...DE,DF. For a board address of A000, the I/O addresses are: A0, A1, A2...AE, AF.

☑ The two jumpers in the upper right-hand corner next to pins 1 and 2 of IC pad 45, the serial port, should be installed if there are no immediate plans for connection to a Modem.



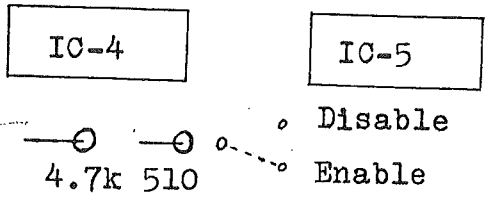
Jumpers for $\overline{CTS}$, $\overline{DCD}$

When used, $\overline{CTS}$ (Clear To Send) and $\overline{DCD}$ (Data Carrier Detect) must be converted to RS-232 levels (they are TTL compatible) using a 1489 or equivalent RS-232 line receiver.



Typical 1489 circuit

Reset-Jump Jumper



IC-4 and 5 are located in the lower left portion of the SCI board.

The reset-jump circuit takes control of the S-100 bus when the reset line (pin 75 on the bus) is active (low). No other jump circuits should be active, as they will probably conflict and the system will hang-up.

This circuit is enabled by placing a jumper from the reset-jump pad to the enable pad. It is disabled by placing a jumper to the disable pad.

The address to which the processor jumps is determined by the first three bytes of the 2708 in IC position 17 (PØ). With the SCI monitor, the jump address is directed to the initialization routine of the monitor, and is typically:

HØØØ	C3	Jump instruction for CPU
HØØ1	1E	Low-order jump address
HØØ2	HØ	High-order jump address

The manner in which the SCI jump circuit is set up requires that the CPU jump to a location within the first 1k of the SCI board address to reset the jump circuit. This design eliminates false reset of the reset-jump circuit when the SCI is addressed at FØØØ. Thus, if other than the SCI monitor is used, and a jump outside the first 1k of the SCI memory block is desired, a second jump instruction must be used, and could be placed immediately following the first jump instruction.

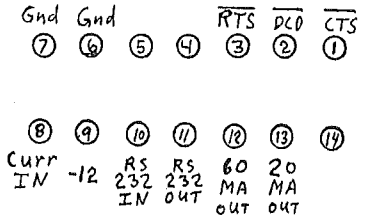
Example: SCI addressed for DØØØ-DFFF, desired jump address is to EØØØ:

DØØØ C3 Ø3 DØ first jump instruction

If a Modem is to be used, the $\overline{CTS}$ and $\overline{DCD}$ (Clear to Send, Data Carrier Detect) from the 1489 will connect to pins 1 and 2 on the interface plug. If a Modem with CTS and DCD is to be used interchangably with a device not sending those signals, wire one I/O plug for the Modem, and another for the other device, connecting pins 1 and 2 to pin 6 on the plug for the other device.

RS-232 or Current Loop

Both an RS-232 device and a current-loop device can be connected to the SCI at the same time. Each keyboard can independently provide input, but each printer will print the same output. The devices must operate at the same baud rate. If only one device is used, the other input must be jumpered on the 14 pin connection plug.



Serial Port Connections
$\overline{RTS}$ is a TTL level output

If a current loop device is used, connect the printer + lead to pin 13 for a 20 ma loop, or to pin 12 for a 60 ma loop, and the other lead to pin 6. The keyboard contacts connect to pins 8 (+) and 7 . The RS-232 input must be jumpered from pin 10 to pin 9.

If an RS-232 device is used, connect the printer lead to pin 11, and the keyboard to pin 10, with common signal lead to pin 7. De-activate the current loop keyboard contact with a jumper from pin 8 to pin 7.

Remember, when only one keyboard device is used on the serial port, the other must be de-activated with an appropriate jumper.

It is recommended that coaxial cable such as RG-174 be used for connection to the serial devices, as the shielding prevents extraneous noise pick-up.

EIA RS-232 Connections

The following page lists the pin numbers used on the EIA RS-232 standard connections. RS-232 is normally used on Modems, and data terminals, for high-speed serial data transfers. The standard connector used is a 25 pin EIA designated type. The use of cables under 50 feet is recommended. If longer cables are used, the total capacitance of the cable and terminator must not exceed 2500 picofarads (micro-micro-farad). Normal cable capacitance is about 30 picofarads per foot.

EIA Connections

The following are the standard connections used with a 25-pin EIA port connector (RS-232).

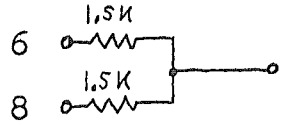
EIA pin	Signal	SCI pin on pad 45	Description
1	Frame ground	--	Connect to chassis ground (Tie to bolt of EIA socket).
2	Terminal Out	10	Data from terminal keyboard.
3	Terminal In	11	Data to terminal printer.
4	Request to Send	--	Request by terminal to send.
5	Clear to Send	--	Send data.
6	Data Set Ready	--	To terminal. If needed, tie to +12 volts through a 1.5k resistor.
7	Signal ground	7	ground, common signal.
8	Received line signal detector		If needed, tie to +12 volts via 1.5k resistor.
9-16	Not used		
17	TTY output	8	Keyboard of TTY serial loop. (Tie to pin 6 if not used.)
18-22	No connection		
24	TTY output	6	ground for TTY loop.
23	TTY input	13	20ma current loop to TTY printer.
25	TTY input	6	ground reference for loop.

If the RS-232 input is not used (SCI pin 10), tie to -12 volts on pin 9.

If the serial input to the SCI is not used, tie pin 8 to pin 6 or 7.

Resistor connections to +12 volts if Data Set Ready or Received Line Signal Detector are needed by terminal:

EIA pin SCI pin (connect to +12 with a jumper).



On SCI, jumper pin 4 (IC pad 45) to pin 8 of IC-38, the LM-358, or TL-082.

Keyboard and Parallel Port Wiring

All three parallel ports are wired identically, except that IC pad 44, the "Keyboard" port, has -12 volts supplied on pin 1, for keyboards that require a negative. bias. Otherwise the ports are identical, and the software determines which ports are input or output. The current available on the +5 volt supply is mainly a function of the regulator temperature. If forced air cooling is used, the regulator will remain cool, and a total of 500 ma is available. If convection cooling is used, it is recommended that total current be held to 100 ma.

If a keyboard is used that has only seven data lines, don't use D7, leave it open.

Gnd D6 D7 SO SI -12 (44)

7 6 5 4 3 2 1 Parallel Ports, 42, 43, 44

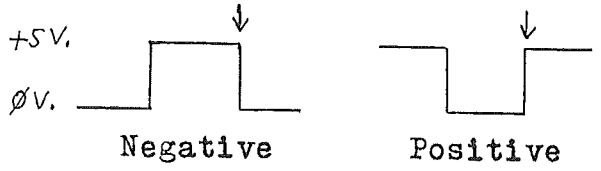
8 9 10 11 12 13 14

D5 D4 D3 D2 D1 D0 +5

DØ-D7= Data lines

SI= Strobe in SO= Strobe out

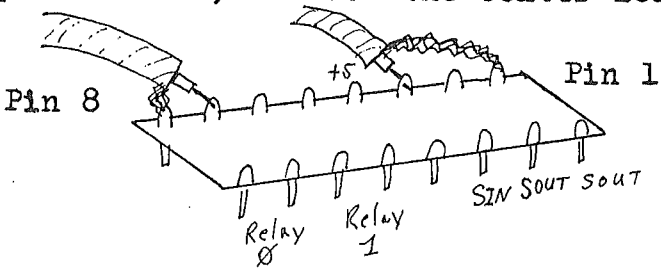
Strobe polarity is determined by software, and is normally negative. The 2k monitor supplied looks at DIP switch 7 to determine the strobe of the Keyboard port. If switch 7 is on, the monitor expects a negative strobe. If the switch is off or "Open", the monitor expects a positive strobe.



Typical Strobe Pulses

Cassette Cable Connections

☒ Cut the audio cable into two equal lengths. These ends then solder to appropriate pins of a 16 pin DIP plug for record and playback connections. If a standard cassette recorder is being used, connect the lead from the speaker jack to pins 7 and 8 on the plug (pin 8, is the shield connection). If a high-impedance output from a deck is used, connect the center lead to pin 6. For a microphone input, connect to pins 1 and 2 (shield to pin 1). If an AUX input is used, connect the center lead to pin 3.



Cassette Connections
Spkr, AUX shown

Cassette Control

☐ If you plan to use two recorders, connect the Read recorder remote control line to pins 9 and 10 on the plug. Connect the Write recorder remote line to pins 11 and 12. When reading a cassette tape, the Read recorder will be activated, and when writing a tape, the Write recorder will be active.

If you will be using one recorder for both reading and writing, wire pin 9 to pin 11, and pin 10 to pin 12. Then connect the recorder remote line to pins 11 and 12, and it will be active when reading and writing.

When using more sophisticated cassette control, pins 14,15, and 16, provide additional control and status lines. Normally, with the monitor supplied, pin 14 is set for status input , for turns counters, or other status info, and pins 15 & 16 output for additional control, connecting to a transistor relay driver or equivalent. These lines can be set up for other configurations, such as all outputs or two outputs and one input, by changing the initialization routine as desired. Complete control of an automatic deck, such as a Phi-Deck, can be easily implemented, to control forward, reverse, read, and write. One status output controls Fast-Forward, or Rewind, one status output controls Read-Write, one on-board relay turns power on and off to the drive motors, and the other

relay controls the Playback-Record solenoid. The status input counts the turns of the tape reel to locate files. Further information is forth-coming.

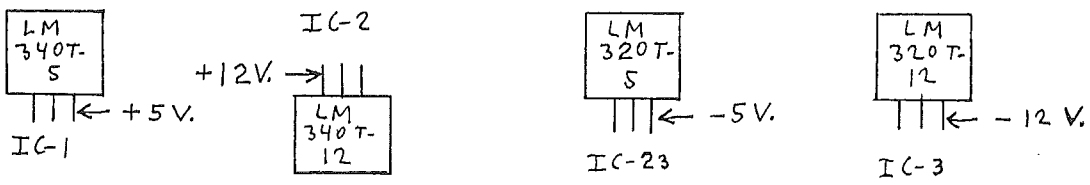
Check-out

Before inserting the I.C.'s or applying power, inspect the finished board. Are all connections soldered, are there any solder bridges ? Are any leads touching other leads ? Solder bridges are not likely to occur with the solder-masked p.c. board. If they do, draw the solder away with the tip of the iron. Compare the orientation of capacitors, diodes, transistors, and sockets, with the layout drawing. Correct any discrepancies. Excess solder flux can be removed with Miller-Stephenson Heavy Duty Flux Remover. Alternatively, isopropyl alcohol and a clean rag will remove flux. Soak a corner of the rag in the alcohol and wipe the flux off, in a direction away from the edge connector, as flux remaining on the connector fingers could cause intermittent connection.

After inspecting and cleaning the board, use a VOM (Volt Ohm Meter) set to resistance scale X 100, to check the resistance of all fingers of the edge connector to ground, pins 50 and 100, and to +5 volts on board (pin 16 of IC 5 or IC 7). This eliminates the destruction of bus drivers in the computer if a problem exists. Most fingers will have infinite resistance.. Zero, or low resistance indicates a problem. Only pins 2 (+16), 52 (-16), and Reset pin 75 will have any resistance indication. Even here, the resistance should be greater than 200 ohms. Of course, pins 1 and 51 the +8 supply will show resistance to ground and to the on-board +5 supply. If there is an abnormal indication, or short, follow the p.c. trace from that finger and look for a solder bridge or an etch problem. Repair the problem.

Caution: never insert or remove a board in the system bus with the power on. Always turn the power off, and wait half a minute for the power supply capacitors to discharge.

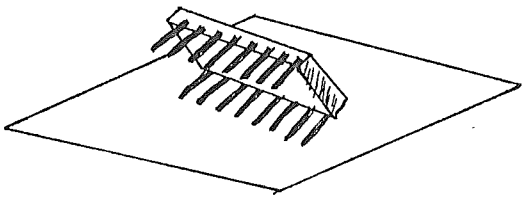
After a satisfactory resistance check, plug the SCI into the system bus and apply power. Measure the voltages out of the four regulators. The values should be within 10 % of the nominal value shown:



If any voltage measurement is not within range, there may be a problem with the regulator, associated bypass capacitor, a short in the p.c. power trace, or inadequate supply voltage. If the regulator is getting very hot, there is probably a short. Check that the associated tantalum bypass capacitors are correctly installed, the + lead is aligned with the + mark on the P.C. board. Or there is a short somewhere from the output trace to ground. If the

regulator is cool to the touch, check the supply voltage to the regulator. If the supply is ok (+8,+16, or -16), the regulator is faulty. Contact DAJEN for a replacement.

☑ With the regulators working correctly, turn off the power and remove the SCI. The next step is to insert the I.C.'s. Be careful when handling the I.C.'s. Avoid conditions that can generate static electricity: don't walk across carpets and then touch the I.C.'s, ground yourself to a metal object such as a desk or chair. Don't slide across plastic covered chairs. Leave the I.C.'s in the pink anti-static plastic bags until actually installing them. Place the p.c. board in front of you, the bag of I.C.'s to one side, and the layout picture to the other side. Remove one I.C. from the bag at a time and install it. Prior to inserting each I.C., straighten any bent pins, and squeeze them in slightly so they line up with the lead receptacles of the socket. One way to do this is to hold the I.C. between thumb and fore-finger, and with the leads resting on a table top, press down lightly. Forming the leads prevents damage to the I.C. pins and to the socket.



To insert the I.C., place the pins directly over the socket receptacles and with an even pressure press the IC into the socket until it seats firmly. The 24 pin I.C.'s will require a great deal of force to seat into the socket.

☑ Note: the 2708 marked P0 plugs into the left-most standard profile socket. P1 plugs into the middle socket, and P2, when supplied, plugs into the right-hand socket(IC-19).

☑ After all the I.C.'s have been installed, make a visual check of their orientation and location. For all vertical I.C.'s, the orientation mark faces toward the top of the board, and for all horizontal I.C.'s the orientation mark faces to the right of the board. Make sure all I.C.'s are in their correct position.

Power-on Test

Plug the completed board into the system bus. Connect the various peripherals (Tape recorder, keyboard, teletype, etc). If you are using a video monitor as the principal console output device, connect to the video interface board in the bus, and turn on the monitor. If you specified a teletype or serial device as the main console output, turn it to "Line". Apply power to the computer. If you have a front panel, hit the "Reset" switch. The front panel lights should indicate address 0000, and the data bus should show C3 (bits 7,6,1,0 on). Hit "Run", the data lights should all glow, and the high-order address lights (A-15,14,13,12) should indicate the address of the SCI board (For example, for address D000, A-15,14, and 12 on, A-13 off). If you don't have a

front panel, hit "Reset". When running, the SCI monitor program clears the video monitor screen, outputs a prompt character (>) to the main console output device, and waits for a command from the main console input device. Characters typed on the input device are echoed to the output device. This action confirms that 90 % of the SCI is functional, so proceed to the Cassette Checkout.

If SCI fails to perform up to here, there is a problem. A few tests can be performed with a voltmeter. To know where to begin, analyze what is happening: when "Reset" is pressed the reset-jump circuit is activated. SCI grabs the bus and outputs a jump instruction to the processor (the jump instruction is the first three bytes in Prom 0). The CPU reads the jump data and jumps to the beginning of the SCI monitor. At this time the reset-jump circuit is reset and the SCI monitor initializes the LSI circuits on board, clears the video screen, outputs the prompt character, and waits for input. Troubleshooting determines where the chain of events is interrupted. This then identifies the area of the faulty component. Start with the reset-jump circuit. With a VOM measure the voltage to circuit ground (pin 7, IC-4) of pin 6 on IC-4, while holding the reset button pressed. This voltage should be less than 0.3 volt. Still holding reset, check the voltage at pin 6 of IC-13, which should be low (0.3), check pin 6 of IC-27, also low, and finally, check the voltage on the DI pins of the edge connector. DI-7,6,1,0, should be high (3 volts or so), and DI-5,4,3,2 should be low. Use the schematic to identify the pin numbers of the DI lines. A problem at this point isolates the reset-jump circuit (IC-4,13,27) or the bus driver IC-10. Tests beyond this point require a front panel and an oscilloscope to trace signals. Contact us immediately.

Programmer

The on-board programmer power supply is active when the switch marked "P" is off or open. Place this switch off. Measure the output voltage at E of the 2N3906 transistor next to IC-29. It should be about 27 volts or slightly higher. Place the switch back in the on position.

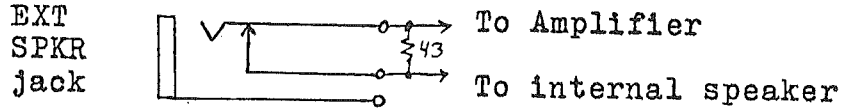
When programming 2708's, switch "P" must be in the off position, otherwise leave it in the on position.

Cassette Check-out

With SCI functioning and responding to commands, insert the supplied tape into the cassette recorder. Turn the recorder volume control to about 1/3 of full range, and the tone control to mid-range. Hit the reset button and type in the command: SR 03E8(CR) (CR=Carriage Return). This sets the cassette read speed to 1500 baud. Place the recorder in the playback mode and type RC(CR) on the keyboard. The recorder should start playing and when the leader tone on the tape is reached, the "Level" light on SCI should glow. Adjust the level of the recorder to illuminate the "Level" light. When the sync code is received, the "Sync"

light will glow. If it doesn't, change switch "R" to the opposite of its present position and repeat the entire procedure from the beginning.

For recorders that can't monitor the tape with a plug in the external speaker jack, add a 43 ohm resistor across the amp and speaker leads as shown:



With the Read circuit working, fast forward the tape to a blank area. Record the digital counter reading. Hit the reset button and use the Z command as follows: Z 0 800 E6(CR). This writes sync bytes into the first 2k of memory. Place the recorder in the record mode and type in this command: WC 0 800(CR). The recorder should start, and then stop after about 10 seconds. Rewind the tape to the beginning of this section, place the recorder in the playback mode, and read in the data. The sync light should glow. If it doesn't glow with sync bytes coming from the recorder, try reversing the "R" switch, hitting reset, and read in the sync bytes again. If they read in this time, return the "R" switch to its original position and flip the "X" switch to the opposite of its present position. This reverses the phase of the data recorded on the tape so it will read in.

Try recording some random memory blocks to check for errors on playback. If there are errors, try adjusting the tone control on the recorder to eliminate them. On some recorders there is an optimum setting of tone for best results.

Tape

We recommend Scotch "Highlander" or AVC series tape, which is low noise, high density, and costs around one to two dollars per 60 minute cassette. With this tape, we estimate an error rate of about one in ten million. We have never had a non-recoverable error (re-reading fails to bring correct data).

Recorders

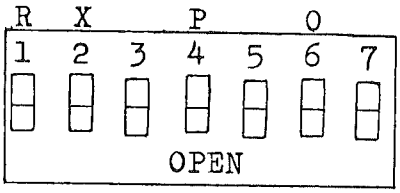
We believe you get what you pay for. A medium-priced recorder will provide better reliability, capability, and much longer life. For a moderately priced recorder, we recommend the Panasonic RQ-430S, at about $50-$60. For best price-performance, we have found the Superscope C-104 at $80-$100 unbeatable. This recorder can routinely record reliably at 5000 baud (624 bytes per second). We have one that's seen continuous service for a year and a half and still provides reliable, fast data recording.

Characteristics to look for in a recorder: a digital tape counter to keep track of program locations, automatic level to eliminate guess-work about recording, freedom from line-noise pick-up. This last requirement can only be deter-

mined by actual use with your system. When you buy a recorder, buy it on condition that you can return it in exchange for one that works with your computer system. Most dealers are willing to comply with your desires. If yours won't, find one who deserves your business.

Maintenance is essential for reliable performance. Keep the tape heads and capstan pressure roller clean. A Q-tip soaked in isopropyl alcohol is a good tool to get to those hard-to-reach places in the recorder. The dirt you see on the cotton swab can cause drop-outs and lost data. Keeping the capstan roller clean will help keep wow and flutter down. Although the SCI cassette interface can tolerate a 33% change in speed, a dirty pressure roller can cause that amount of speed change and consequent loss of data. We routinely record 24k data blocks, and following the above precautions, we almost never have errors.

DIP Switch Functions



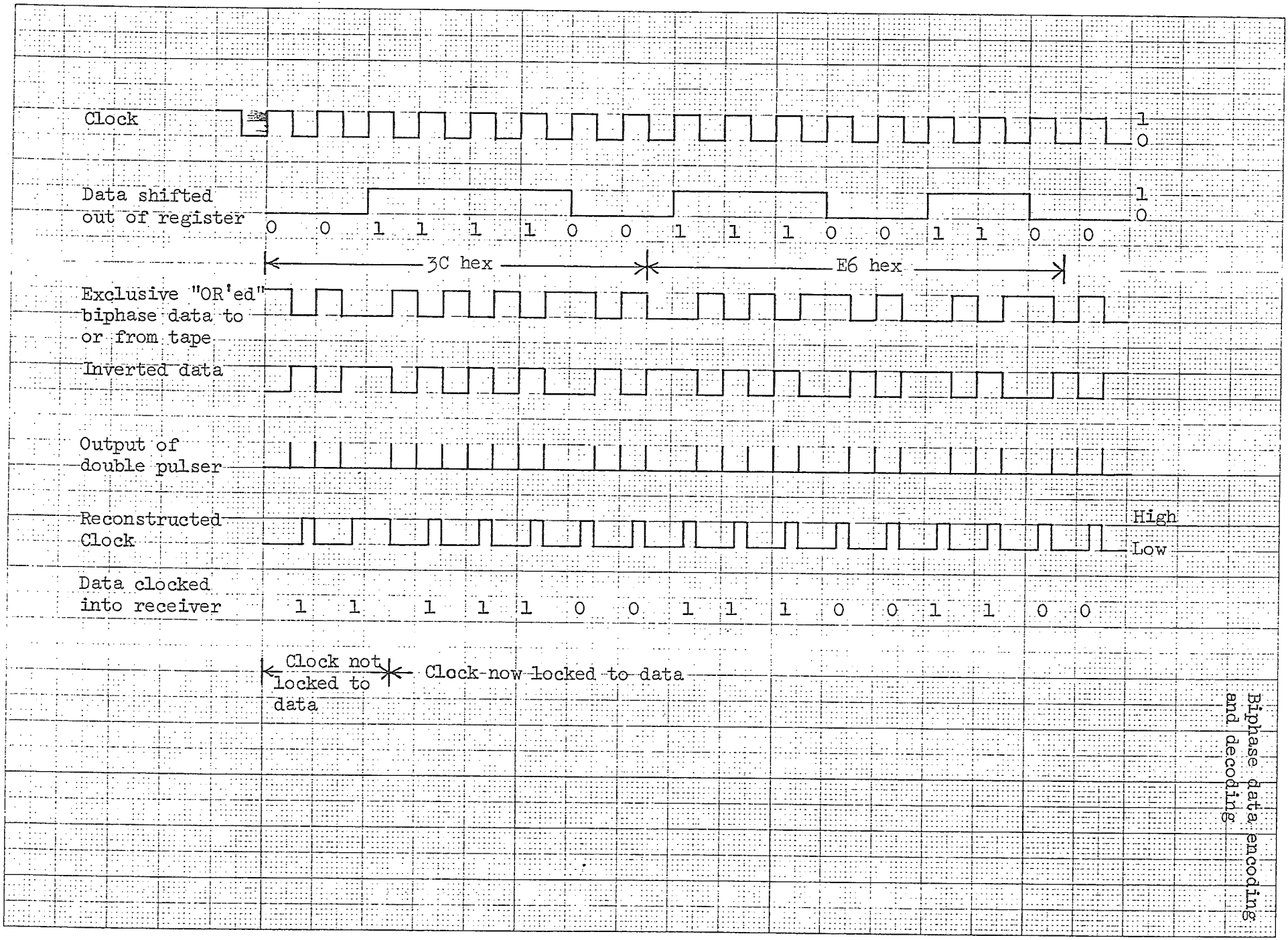
DIP Switch in IC pad 39

Switches 1 and 2 control the data inversion in the biphase cassette interface. Switch 1, "R", inverts the received data from the tape recorder. Switch 2, "X", inverts the data transmitted to the recorder. These switches compensate for different data inversions in different recorders.

Switches 3 and 5 are not used, and are available to the user if so desired.

Switch 4, "P", is the Programmer enable switch. When "OPEN" or "OFF", the on-board 2708 programmer is active. Normally, except when programming 2708's, this switch is "ON" to prevent inadvertent programming of the 2708 in IC pad 19 (3rd standard profile socket on the right.).

Switches 6 and 7 control options selected by the SCI monitor program. In current versions of the SCI software, switch 6, on initial start-up or reset, selects the console devices used for input and output. When switch 6 is "ON", a keyboard connected to IC pad 44 is assumed to be the console input device, and a video interface is assumed for output. When switch 6 is "OPEN" or "OFF", a serial device connected to IC pad 45 is assumed for both input and output.



Biphase data encoding and decoding

Theory of Biphase Cassette Operation

Biphase recording is a means of recording digital data in a high-speed, densely-packed format, on cassette tape. Because each cycle of the recording process represents one data bit, there is no wasted space. A standard cassette recorder operating well within its capabilities can record data at 2500 baud error-free. This is 2500/8, or 312 bytes per second. In comparison, Kansas-City recording, operating with shifting frequencies, runs at 300 baud, or 37 bytes per second. Thus biphase is faster, and can as a consequence store more data on a given cassette. A 30 minute side of a standard Phillips cassette can hold 500 k-bytes of data.

To understand how biphase works, look at the figure on page 12 titled "Biphase Data Encoding and Decoding". Look at the top drawing. This is the basic cassette clock which sets the data transmission speed, or baud rate (one baud is one bit per second). This clock is generated by dividing the crystal-controlled system clock through a series of dividers. Contained within the cassette interface is a shift register which is loaded with one byte of data to be output. Each positive transition of the cassette clock shifts one bit out ot the shift register. Data in a Tarbell-type system is shifted most significant bit first (bit 7 first, then bit 6, 5, ...1, 0). When all eight bits of the present byte are shifted out, the interface requests another byte.

The data shifted out of the register is then exclusive-OR'ed with the cassette clock. The logic states of a two-input exclusive-OR gate are as follows:

Inputs	A	+	B	=	Y	Output
	0		0		0	
	0		1		1	
	1		0		1	
	1		1		0	

Note: when both inputs are the same, the output is low.

The third line of the figure on page 12 illustrates the data after it has been exclusive-OR'ed with the clock. This is then fed to the recorder input. Notice that when the data is unchanging (a string of zeroes or ones), the output to the recorder is the cassette clock frequency, and when the data changes from a one to a zero, or a zero to a one, an extra one-half clock cycle is added to the data output. These extra half-cycles are the basis of biphase. When they occur, the phase changes and the decoded data changes to the opposite state.

Now consider the decoding process. For the decoder presented, the input data must be inverted to provide the correct data output.

After being amplified and squared by a comparator, the data from the tape recorder is fed to a receiver shift register and a "double pulser". The "double pulser" puts out a pulse every time the incoming data changes state.

This output triggers a digital timer which is set equal to 75% of the time required for one complete cassette clock cycle. The output of this timer is the "reconstructed clock" shown in the figure. When triggered, this timer output goes low until it times out and returns to the high state. As it returns, the timer output pulse clocks the present data bit into the receiver shift register. When eight bits of data have entered the shift register, the cassette interface signals the computer that a data byte is available.

Notice that the first two data bits clocked into the receiver are 1's, where 0's were sent originally. The interface, started at random, has not locked to the data stream. However, after the first data transition from a 0 to a 1, the clock is now locked to the data stream, and the correct bits are entered into the receiver register. That first byte of data (3C hex) is called the clock synchronizing byte, because it synchronizes the reconstructed clock with the data stream.

The byte following the clock sync byte, is the data synchronizing byte (E6 hex). Up to the time it is received, the receiver shift register has been reset, not signalling the reception of bytes to the computer. When the receiver recognizes the data "sync" byte, it knows the next 8 bits will be a data byte, and readies the data flag to signal the computer that a data byte is available.

Analyze what would happen if the original, non-inverted data had been input to the receiver: all the data would be inverted. This is why the receiver has a data inversion switch. If the tape recorder doesn't invert the data it receives, then the interface must.

The reason there is a transmitted data inversion switch is to allow easy software interchange among biphase-system owners. Each interface is shipped with a pre-recorded cassette tape. The system owner adjusts his interface and recorder to be compatible with that tape and he is then able to easily exchange tapes with other owners.

Parts List

Capacitors

3	39 pf
2	.001 uf
4	.0047uf
3	.01 uf
4	.05 uf
16	4.7uf 35 VDC

Resistors 1/4 watt, unless noted

4	4.7 ohm	(Yellow-Violet-Gold)
3	20 1/2 watt	(Red-Black-Black)
1	51 1/2 watt	(Green-Brown-Black)
2	43	(Yellow-Orange-Black)
2	300	(Orange-Black-Brown)
1	300 1/2 watt	(Orange-Black-Brown)
6	510	(Green-Brown-Brown)
1	510 1/2 watt	(Green-Brown-Brown)
10	2k	(Red-Black-Red)
28	4.7k	(Yellow-Violet-Red)
5	20k	(Red-Black-Orange)
2	39k	(Orange-White-Orange)
3	100k	(Brown-Black-Yellow)
1	1Meg	(Brown-Black-Green)

6	1N4148 diodes
2	MV-5075 LED lights
4	2N3904 transistor
3	2N3906 transistor
1	MJE 180 transistor
1	7-pole DIP switch
4	14 pin DIP plugs
1	16 pin DIP plug

Sockets

3	8 pin
15	14 pin
10	16 pin
3	20 pin
3	24 pin low profile
3	24 pin standard profile
2	40 pin

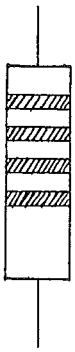
2 Heat Sinks

I.C.'s

2	74LS00	1	LM-320-T5
2	74LS04	1	LM-320-T 12
2	74LS11	1	LM-340-T 5
1	74LS32	1	LM-340-T 12
2	74LS155	1	LM-358
2	74LS221	1	LM-380
2	74LS367	2	LM-2903
1	74LS386		
2	2112		
2	2708	1	Audio Cable
2	6820	1	Cassette tape
1	6850		with Sync code
1	6852	1	P.C. Board
1	8131	4	4-40 bolts and nuts
3	81LS97	15	feet of solder
1	8253		

Polarity mark on tantalum cap's

Resistors

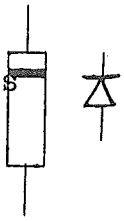


1st color
2nd color
3rd color
gold or silver

1/2 watt is larger than 1/4 watt res.

Diodes

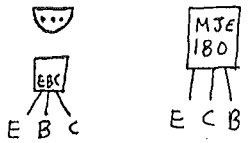
LED's



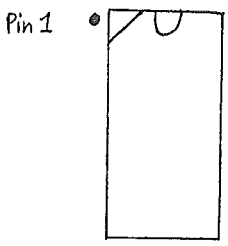
Band indicates cathode

Flat indicates cathode

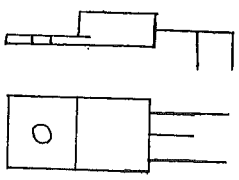
Transistors



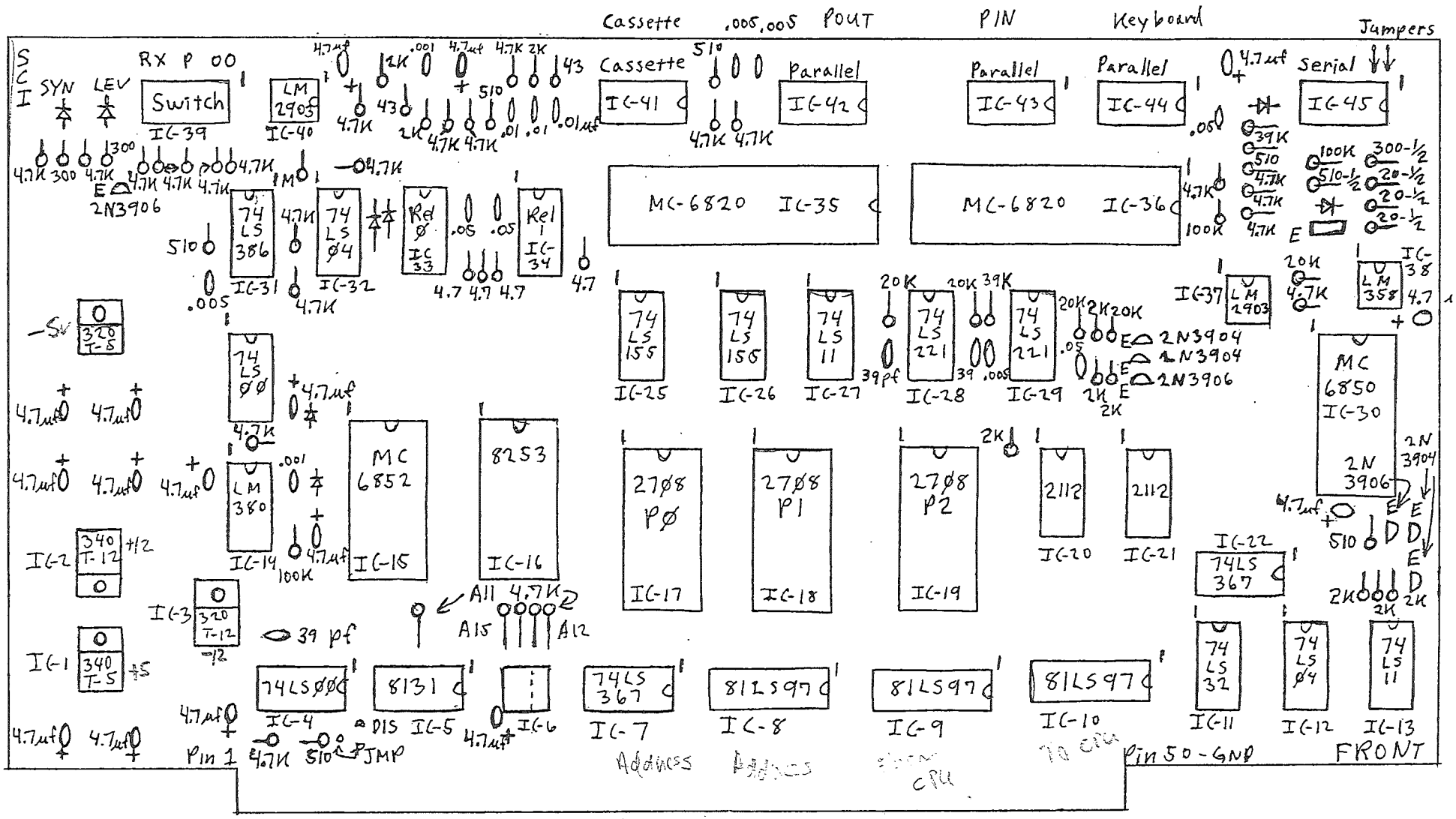
I.C.'s and sockets



A notch or dot or U section locates pin 1



Typical Regulator Installation



B2
Parts Layout

Baud Rate Table

This table lists some of the baud rates which the cassette and serial ports can generate. Use the appropriate command (SR for Read, SS for serial, SW for write) to set the desired baud rate by inserting the hex number listed in the table, after the command letters. For example, to set the Read speed for 3600 baud, the command is: SR 01A0 CR (Carriage Return). Remember that when reset, or started cold, the various speeds are set by the pre-determined values in the initialization routine. For speeds not listed in the table, the appropriate hex number can be calculated as follows:

For Write: N=2,000,000/Baud Rate, N must be expressed in hex. Example: 2500 baud desired. N=2,000,000/2500=800 decimal A hex number is N3 N2 N1 N0, where N3 has a value of 4096, N2 256, N1 16, N0 ones. 800 has 0-4096, so N3=0;800 has 3-256, so N2=3. This leaves 800-3X256=32. N1=2 (2X16=32), and N0=0 because nothing remains. Thus the hex number is 0320. The command is: SW 0320CR (Carriage Return).

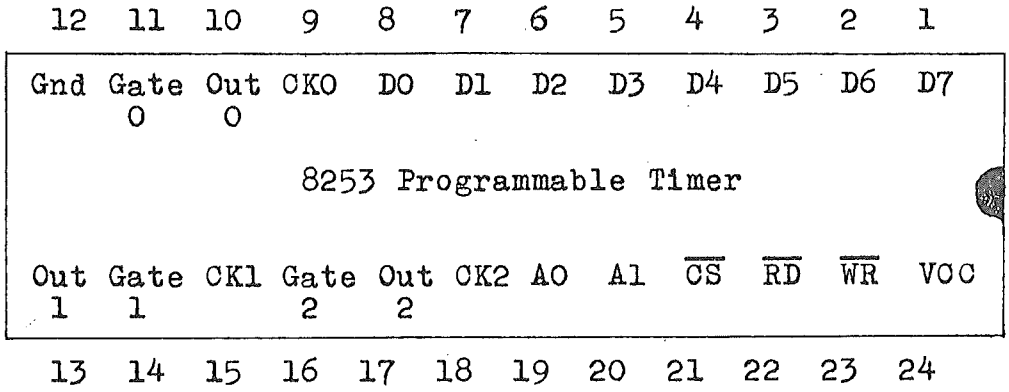
Read speed: N=1,500,000/Baud Rate

Serial speed: N=125,000/Baud Rate

Baud Rate	Cassette System Write	Cassette System Read	Serial Port Serial	
45.45	ABE4	80EB	0ABE	60 WPM, Baudot
75	682A	4E20	0682	
75.75	6722	4D59	0672	110 WPM, Baudot
110	4705	3544	0470	
150	3415	2710	0341	
300	1A0A	1388	01A0	
600	0D05	09C4	00D0	
900	08AE	0682	008A	
1200	0682	04E2	0068	
1500	0535	03E8	0053	Tarbell cassette
1800	0457	0341	0045	
2200	038D	02A9	0038	
2400	0341	0271	0034	
2500	0320	0258	0032	DAJEN Cassette
3000	029A	01F4	0029	
3600	022B	01A0	0022	
4000	01F4	0177	001F	
4800	01A0	0138	001A	
5400	0172	0115	0017	
6000	014D	00FA	0014	
7200	0115	00D0	0011	
8000	00FA	00BB	000F	
9600	00D0	009C	000D	
10400	00C0	0090	000C	
12000	00A6	007D	000A	
14000	008E	006B	0008	
18000	006F	0053	0006	
19200	0068	004E	0006	
31000	0040	0030		
45000	002C	0021		
70000	0010	0015		
100000	0014	000F		

8253 Programmable Timer

Pin Configuration



D0-D7 Data lines
A0,A1 Address lines
CK0,1,2 Clock inputs
$\overline{CS}$ Chip Select
$\overline{RD}$ Read
$\overline{WR}$ Write

The 8253 consists of three independent 16-bit programmable timers, with a maximum count rate of 2 mhz. Each counter is programmed by writing a mode control word into the control word register. Depending on the mode, the count is loaded into the appropriate count register.

Control Word: D7 D6 D5 D4 D3 D2 D1 D0

Bit assigned: SC1 SC0 RL1 RL0 M2 M1 M0 BCD

Where: SC=Select Counter to which control word applies

SC1	SC0	Counter
0	0	0
0	1	1
1	0	2
1	1	Illegal

BCD= 0= Binary counter
1= 4-decade BCD counter

RL=Read/Load command

RL1	RL0	
0	0	Latch counter for read operation
0	1	Read/Load least significant byte only
1	0	Read/Load most significant byte only
1	1	Read/Load least sig.byte first, then most sig.byte.

Mode:

M2	M1	M0	Mode
0	0	0	0
0	0	1	1
X	1	0	2
X	1	1	3
1	0	0	4
1	0	1	5

where X= don't care

Bus Address:

A1	A0	Device Selected
0	0	Count Reg. 0
0	1	Count Reg. 1
1	0	Count Reg. 2
1	1	Control Reg.

8253 Programmable Timer

Mode Definitions

Mode 0: Out will be low at start of count, goes high and remains high at the end of the count. The Gate input inhibits counting when low, and enables counting when high. Out goes low when count register is re-loaded. Re-loading during counting: 1st load byte stops the count, 2nd load byte starts the new count.

Mode 1: Programmable One-shot. Out goes low following the rising edge of the Gate input. Out goes high at the end of the count. If a new count value is loaded during the counting, the current count will not be affected. The One-shot is retriggerable and Out will remain low for the full count after the last trigger.

Mode 2: Rate Generator. Divides by N (the count). Out is low for one period of the input clock after each N counts. Gate when low inhibits counting and holds Out high. When Gate goes high, the counter starts counting for the full count. Gate will synchronize the counter. If the count register is reloaded, only subsequent counts will be affected. When Mode 2 is set, Out remains high until the count is loaded.

Mode 3: Square wave generator. Similar to mode 2, but the output is a square wave. If the count is odd, Out is high for (N+1)/2 counts, and low for (N-1)/2. If the count register is reloaded, the new count is effective immediately after the next output transition. Gate controls counting.

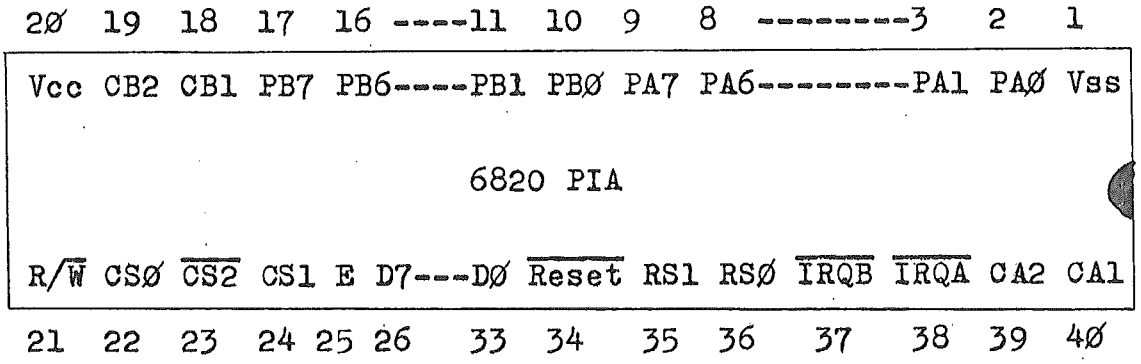
Mode 4: Software triggered strobe. Out is high after the mode is set. When the count is loaded, counting begins. Gate low inhibits counting. On reaching the count, Out goes low for one clock period. Reloading the count register while counting does not affect the present count. Reloading the count register restarts counting. Gate low inhibits counting.

Mode 5: Hardware triggered strobe. The counter starts counting after the rising edge of the Gate input, and Out goes low for one clock period when the count is reached. The counter is retriggerable.

The loading of the count register does not have to immediately follow the loading of the Mode register. The sequence of bytes specified in the mode word must be followed. All counters are down counters (count down from the count loaded).

To read the counter while counting, issue the RL 0 0 mode addressed to the correct counter in a mode word. Then reading the counter will produce a latched count. The mode of reading must then be issued, and either one or two reads made to input the least significant byte, then the most significant byte of the count. The entire reading procedure must be completed. If two bytes are to be read, then two bytes must be read, otherwise the WR command can't be sent to the counter.

6820 Peripheral Interface Adapter



CA1, CA2 Control lines for parallel port A
CB1, CB2 Control lines for parallel port B
CSØ, CS1, CS2 Chip select inputs
DØ-D7 Data bus lines
E Enable pulse, clocks valid data, conditions control lines.
IRQA, IRQB Interrupt flag lines for use in interrupt-driven systems.
PAØ-PA7 Parallel Port A
PBØ-PB7 Parallel Port B
R/W Read/Write control
Reset Resets control registers and flags
RSØ, RS1 Address lines to select internal registers.

The 682Ø Peripheral Interface Adapter consists of two independent parallel ports, each with its own handshake signals and interrupt request line, each bit programmable as input or latched output, and the necessary control registers to implement operation.

Register Addressing

RS1	RSØ	Control Register bit	Location selected
Ø	Ø	CRA-2= 1	Data Register A
Ø	Ø	CRA-2= Ø	Direction Register A
Ø	1		Control Register A
1	Ø	CRB-2= 1	Data Register B
1	Ø	CRB-2= Ø	Direction Register B
1	1		Control Register B

The Data Direction registers determine the function of each bit in the associated parallel port. A Ø bit sets the corresponding peripheral line to an input mode. A 1 results in a latched output mode.

The Control Registers set the operation of the control lines, CA-1,2, CB-1,2, and enable the interrupts. Bits Ø-5 of the control register may be written and read, while bits 6 and 7 are read-only.

Control Word Format for Control Registers

Bit 7	6	5 4 3	2	1 Ø
IRQ1	IRQ2	CA-1 Control CB-1 Control	Data or Direction Register	CA-1 Control CB-1 Control

6820 continued

Bit 2 of each control word allows access to either the data or direction register. See the register addressing on page E-3.

Bits 6 and 7 are read-only flags, and are set by signals on the Control lines. They are reset after read operations, by an E pulse, when the PIA is not selected.

Control lines CA-1,2, and CB-1,2, can be programmed for a variety of input-output functions. The following tables summarize the options available:

Interrupt inputs CA-1 and CB-1

Bit 1	Bit Ø	Interrupt Input	Interrupt Flag Bit 7	Interrupt Request $\overline{IRQA}$ or $\overline{IRQB}$
Ø	Ø	↓ Active	set high	Disabled-$\overline{IRQ}$ stays high
Ø	1	↓ Active	set high	Low when flag goes high
1	Ø	↑ Active	set high	Disabled-$\overline{IRQ}$ stays high
1	1	↑ Active	set high	Low when flag goes high

CA-2 and CB-2 as interrupt inputs

Bit5	Bit4	Bit3	Interrupt Input	Flag Bit 6	Interrupt request $\overline{IRQA}$ or $\overline{IRQB}$
Ø	Ø	Ø	↓ Active	set high	Disabled-$\overline{IRQ}$ stays high
Ø	Ø	1	↓ Active	set high	Low when flag goes high
Ø	1	Ø	↑ Active	set high	Disabled-$\overline{IRQ}$ stays high
Ø	1	1	↑ Active	set high	Low when flag goes high

CB-2 configured as an output

Bit5	Bit4	Bit3	CB-2 Cleared	CB-2 Set
1	Ø	Ø	Low on positive transition of first E pulse after a write B operation.	High when flag bit 7 is set by active transition of CB-1.
1	Ø	1	Low on positive transition of first E pulse after a write B operation.	High on pos. edge of first E pulse after E pulse which occurred when not selected.
1	1	Ø	Low when CR bit 3 goes low after write into Control Register B.	Low as long as CRbit 3 is low. High when CR bit 3 is written high.
1	1	1	same	same

CA-2 configured as an output

1	Ø	Ø	Low on negative transition of E after a read operation of reg A.	High when flag goes high from active transition on CA-1
1	Ø	1	same	High after first E pulse when part not selected

6820 continued

Bit5	Bit4	Bit3	CA-2 Cleared	CA-2 Set
1	1	Ø	Low when CR bit 3 is set low. ('A' Control Register)	High when CR bit 3 is set high ('A' Control Register)
1	1	1	same	same

Parallel Port A has internal pull-up resistors that represent about one TTL load. When configured as outputs, the voltages at the port pins must be above 2.0 volts, or erroneous data will be seen when trying to read what was written.

Parallel Port B when configured as output, can drive up to 1 ma of current, and the output voltage does not have to be above 2.0 volts for the output to be read correctly after a write operation. Thus, Port B can drive the base of a transistor switch directly.

The E pulse conditions the interrupt control lines. At least one E pulse must occur from the inactive edge to the active edge of the input signal to condition the edge sense network. In other words, at least one E pulse (about 2 us apart) must occur between strobe inputs from an external device. Then the interrupt flag will be set on the next active transition of the strobe.

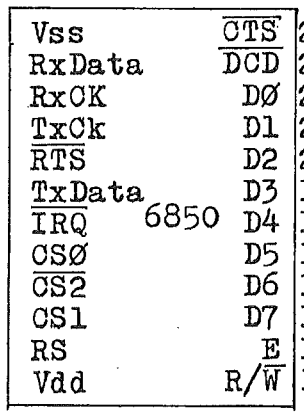
The interrupt flags are cleared after a read of the particular data register. They can not be set again until an E pulse occurs while the part is deselected.

Interrupts

When using interrupts, $\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ is tied to the appropriate Vectored Interrupt pin on the S-100 bus, or they may be tied together to Int (pin 73), as they are open-drain outputs. Then when an interrupt occurs, the appropriate flags can be checked in the Control Registers to determine the requesting device.

6850 Asynchronous Communications Interface Adapter, or ACIA

Pin-outs



Definition of pins

CSØ, CS1, CS2 Chip-select inputs. When CSØ and CS1 are high, and CS2 is low, the 6850 is selected by the bus.

CTS Clear to Send input from a modem, when low indicates that the data channel is ready for transmission. When a modem is not used, must be tied to ground.

DCD Data Carrier Detect input from a modem, when low the data carrier is present. If high, the data carrier is lost, and the 6850 will generate an interrupt to reflect the DCD status in the status register. The receive interrupt must be enabled for this to happen. Must be tied to ground when not used.

DØ-D7 Eight bidirectional data lines to the central bus.

E Enable input. Clocks data to and from the ACIA and enables the input/output bus drivers.

IRQ TTL compatible, open drain, active low output that requests an interrupt when the ACIA interrupts are enabled. It may be tied together with other open-drain interrupt outputs in a polled-interrupt system where the interrupt routine checks the status of each device to determine which one requested service.

RS Register Select. Tied to address line AO. When low, the status/control registers are selected. When high, the receive/transmit data registers are selected.

RTS Ready to Send output. Signals the modem that the ACIA is ready to send data. Active low.

R/W Read/Write signal from the bus.

RxCK Receiver clock, normally 16 times the actual data rate.

RxData Received data, serial input, least significant bit first.

TxCK Transmitter clock, normally 16 times the data rate.

TxData Transmitter data, serial output, least significant bit sent first.

Vss System ground.

Vdd +5 volt supply, nominally 5%.

The ACIA transmits and receives serial data in an asynchronous format, with one start bit, seven or eight data bits, and one or two stop bits, with or without parity. As used in the SCI, the ACIA is set up for one start bit, eight data bits, no parity, two stop bits, and divides the clock by a factor of 16.

Status Register Bit Assignments:

The status register is selected when RS is low, and R/W is high, and the ACIA is selected.

Bit	7	6	5	4	3	2	1	Ø
	IRQ	PE	OVRN	FE	CTS	DCD	TDRE	RDA

CTS Indicates the state of the CTS pin. When high, TDRE is disabled.

DCD Indicates the state of the DCD pin. Remains high after DCD goes low, until reset by reading the status register then the data register, or reset by Master Reset.

FE Framing error which indicates a lack of the proper stop bit, which can be the result of a poor transmission, or the break condition (open loop).

IRQ Interrupt request status, reflects the state of the IRQ pin. High indicates interrupt. Cleared by a read or write data operation.

OVRN Indicates a receiver over-run. The last received data was not read by the time the new data was ready.

PE Parity Error, when parity is selected, indicates that the parity of the received data did not match the parity of the data transmitted, which results from a lost data bit.

RDA Received data available in the receiver buffer.

TDRE Transmit Data Register Empty, ready for new data to be entered for transmission.

Control Register Bit Assignment:

The control register is selected when RS is low, R/W is low, and the ACIA is selected.

Bit 1	Bit Ø	Select Clock divide ratio, or reset
Ø	Ø	Divide by 1
Ø	1	Divide by 16 (SCI)
1	Ø	Divide by 64
1	1	Master Reset

Bit 4	3	2	Word Length, Parity, Stop bits
Ø	Ø	Ø	7 data bits, even parity, 2 stop bits
Ø	Ø	1	7 bits, odd parity, 2 stop bits
Ø	1	Ø	7 bits, even parity, 1 stop bit
Ø	1	1	7 bits, odd parity, 1 stop bit
1	Ø	Ø	8 bits, 2 stop bits (SCI)
1	Ø	1	8 bits, 1 stop bit
1	1	Ø	8 bits, even parity, 1 stop bit
1	1	1	8 bits, odd parity, 1 stop bit

Bit 6	5	State of RTS	Transmit control
0	0	low	transmit interrupt disabled
0	1	low	interrupt enabled
1	0	high	interrupt disabled
1	1	low	interrupt disabled, break level (open loop) transmitted.

Bit 7 Receive interrupt control

0	disabled
1	enabled

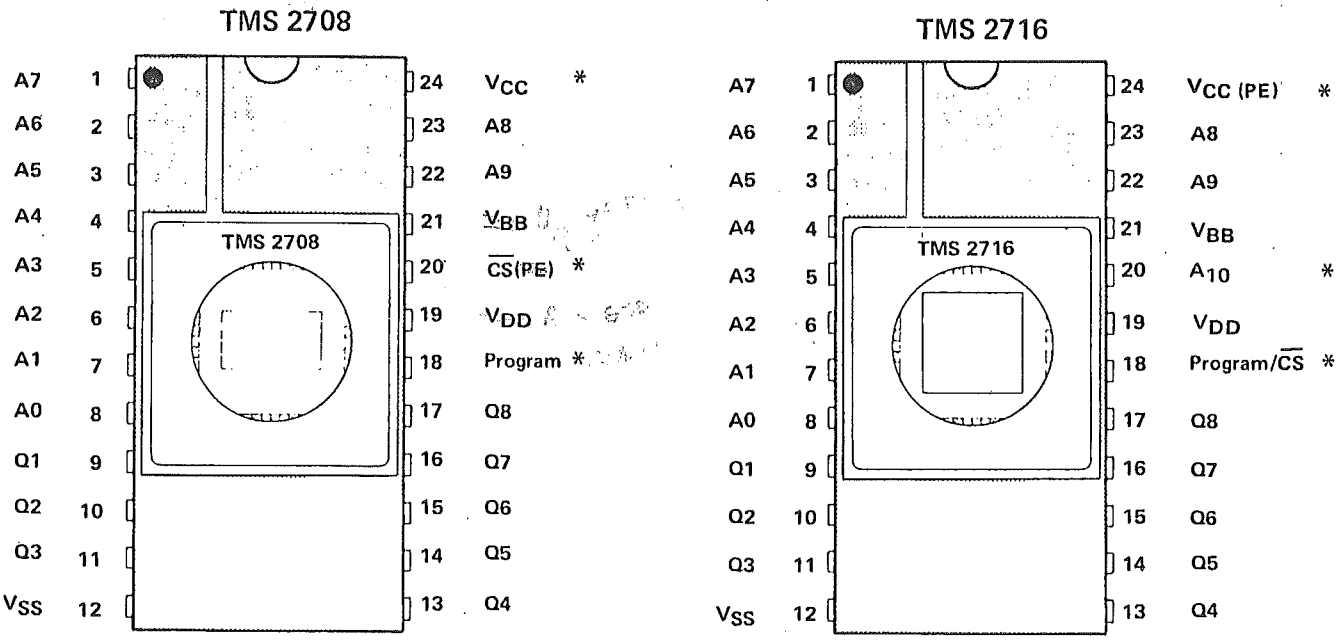
APPLICATIONS INFORMATION

Ease of Conversion From TMS 2708 To TMS 2716

A. The TMS 2716 and TMS 2708 have compatible timing, voltage and current parameters in both modes.

B. The 2716 requires less power than the 2708.

C. The pinouts are compatible. (See below.)



As can be seen from the above diagrams, only three pins* are modified in going from TMS 2708 to TMS 2716:

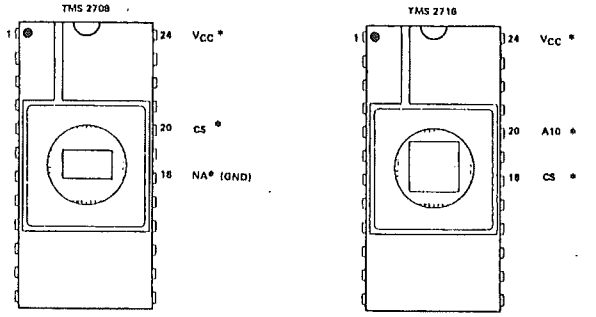
1. The additional address pin required for the 16K EPROM is located on pin 20 which displaces the $\overline{CS}$/PE functions on the 2708.

2. Since V_{CC} is not required during programming, the PE function shares pin 24 with V_{CC}.

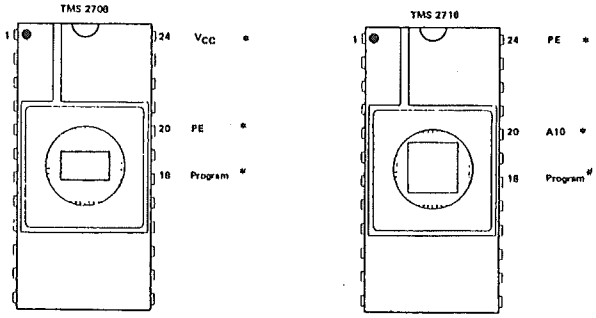
3. The $\overline{CS}$ function and program function are mutually exclusive during normal read mode (and are self-actuated complementary during the program/verify mode) and share pin 18.

The diagrams below show how these three pins are actually utilized in the read mode and in the program mode. Only pins 18, 20, and 24 need to be shown, as all other pin connections are identical.

Read Mode



Program (Write) Mode



TMS 2716 — Easy Programmability On Existing 2708 Programmers

All timing, voltage and current parameters are compatible so that existing 2708 programmers can easily and simply be converted to program the TMS 2716.

A simple cost-effective method to program the TMS 2716 on existing TMS 2708 programmers with no modification to the existing programmer is discussed in a separate application brief. All that is required is two switches and two sockets to allow each 8K half of the TMS 2716 to be programmed/verified separately.

Existing EPROM Programmers — Upgrading To the TMS 2716

Most of the EPROM manufacturers are in the process of implementing field upgrade modifications to allow TMS 2716 programming on current EPROM programmers. This is greatly simplified because the TMS 2716 and the TMS 2708 are programmed in an identical manner. A slight modification to the socket card, an additional 1K x 8 of RAM, and an extra address signal (A10) are all that is required. All timing and voltage parameters are identical, so the upgrade is easily accomplished. Programmer manufacturers contacted to date on the TMS 2716 include: Data I/O, PRO LOG, Texas Instruments, Technico, CramerKit, Shepardson Micro Systems, Cromenco, MicroPro, and Ramtek.

Reference information

For further information on the 8253 Programmable Counter, see the Intel Data Catalog
Intel Corporation
3065 Bowers Ave.
Santa Clara, Ca 95051

For information on the 6820, 6850, and 6852, see the M6800 Microcomputer System Design Data from:
Motorola Semiconductor Products, Inc
Box 20912
Phoenix, Arizona 85036

A good source of data for TTL IC's is:

The TTL Data Book for Design Engineers

Texas Instruments, Inc.
P.O. Box 5012
Dallas, Texas 75222

SCI 2K Monitor version 1.5

This monitor provides the routines that initialize and interface the LSI circuits on board the System Central Interface. Other monitor functions are a video driver for a video display interface, commands to display and alter memory, high-speed cassette routines to store and load blocks of memory or data in a check-summed format (Automatically starting and stopping the tape recorders), assign I/O devices, and program 2708's.

Monitor Operation

When reset is activated, or on initial start-up, the monitor configures the I/O ports, sets the speeds for cassette and serial port operation, and turns off the relays. The monitor then erases the screen of the video display, clears the command buffer area, outputs a prompt character (>) to the main console output device, and waits for a command.

Commands consist of one or two letters followed by hexadecimal addresses where appropriate. Command letters must be followed by a space, then addresses as necessary. If a mistake is made when typing in a command, hit rubout or control H (backspace) to delete the last character typed. Addresses can be from one to four hex characters (Ø-9,A-F). If more than four hex characters are typed without any intervening space, only the last four characters will be used. For example, if AC1ØØ is typed, only C1ØØ is seen by the monitor. To read 16 bytes of a tape, and place them at ØØØØ hex, the following is sufficient: RS Ø 1Ø (CR).

All command strings are terminated by a carriage return. At this time, a line feed and carriage return are output, and the command is executed. If the command is erroneous, or there is an error in the command string, ERROR is output and the monitor waits for a new command. After the command has been executed, an appropriate remark is output and the monitor awaits another command.

Escape

All command routines contain an escape. To return to the command mode, just hit the Escape (Esc) key on the main console input device. The routine being executed will abort, and the monitor will wait for a command input. When escape is used to exit cassette routines, the cassette relays are left activated. This allows the operator to rewind, or fast forward the cassette. Before using the cassette routines again, the reset switch must be activated, or a command to go to the start of the monitor. This re-initializes the cassette ports and turns the relays off.

Video Driver Software

This driver assumes that the video interface is a 1k block of memory located at CCØØ to CFFF hex, and that CCØØ is the upper left-hand corner of the monitor screen. A cursor is displayed on-screen to indicate where the next character will be written. Control commands available are: carriage return, which moves the cursor to [illegible]

hand margin; line feed, which moves the cursor down one line; control H, a backspace, which moves the cursor back one position (when the cursor is at the left-hand margin, backspace moves it to the right-hand margin, one line up); rubout, does the same thing as backspace; control K, a vertical tab, moves the cursor to the upper left-hand corner of the screen (useful for live-action games, the program can use the upper left corner as a reference point to the rest of the screen when changing parts of the display); control L, form feed, which erases the entire screen and places the cursor at the upper left corner of the screen.

When the last line of the display is filled, the screen is scrolled up one line. The speed at which this occurs can be varied by typing Ø-9 during the scrolling process. Ø is the slowest speed, about 2 seconds per line, and 9 is the fastest, about 1Ø lines per second. Typing a space will stop the scroll. Typing any other character will start it again.

There are differences among the video interfaces offered on the market. The P-Tech VDM requires that bit 7 be low for characters output to the screen. The Poly VTI requires bit 7 be high. The areas where bit 7 is critical are illustrated in the video driver section of the assembly listing.

Jump Locations

At the beginning of the monitor are 12 jump instructions. The first jump simply jumps to the start of the monitor. The following jumps are the solution to easy interfacing with any program. Just call the appropriate routine and the SCI monitor takes over to do all the interface work. No need to worry about port locations, status data, or cassette routines. Each call (3 bytes) replaces at least 10 bytes in a typical status check, data handling routine, and the 12 bytes of cassette functions replace at least 38 bytes of code, in addition to providing much more advanced functioning. So program modification is simple, fast, and saves memory space.

Data in the routines is always handled in the accumulator (A). H is the high-order nibble of the SCI memory location (example, DØØØ, EØØØ, FØØØ, etc.).

HØØ3 Jumps to the input routine and returns to the calling program with the character from the console input device. Bit 7 is not masked.

HØØ6 Jumps to the console output routine, outputs the character, then returns.

HØØ9 Cassette input. Calling this location starts the recorder, waits for a level indication, initializes the cassette circuits, and returns with a data byte. Each subsequent call returns with a byte of data.

HØØC End cassette read operation. Call this location when all the data has been read. This routine then waits for an inter-record gap (a blank spot), then turns off the recorder.

HØØF Cassette write. This routine turns on the recorder, writes a leader on tape, sets the baud rate, outputs

the sync bytes then the data. Subsequent calls will write data to tape.

HØ12 Cassette write end, writes a brief trailer, followed by an inter-record gap, turns off the recorder, and returns to the calling program.

HØ15 Parallel input from the second parallel input port. (Port HØ). Gets the data byte and returns. Useful for paper tape readers or analog-to-digital converters.

HØ18 Parallel output, port H6. Outputs a byte, then a strobe pulse to the peripheral, and returns.

HØ1B Input status check. The status of the currently-selected input device is polled. If data is not available, the zero flag is set. If data is available, the zero flag is not set, and the accumulator will return with the data byte. This is useful for escape routines, data input, and is directly compatible with Processor Technology software. Bit 7 is masked low on all data (E6 7F).

HØ1E Input masked. This routine is identical to HØØ3, but masks bit 7 low for all data. Saves two bytes in the user's program.

HØ21 Write B. This routine outputs the data byte passed in the B register. Directly compatible with Processor Technology software.

For details on the use of these jump locations, and interfacing the SCI to popular software, see appendix H, "Patches to Popular Software".

Cassette Format

The cassette tapes written and read by this monitor have the following format: a leader of tone, a clock synchronizing byte (3C hex), a data synchronizing byte (E6 hex), a low-order starting address byte (where the data will be stored), a high-order starting address byte, a high-order block-length byte, a low-order block-length byte (the number of data bytes), the data, and a checksum which is the 8-bit result of adding all the bytes (excluding the clock and data sync bytes), and finally a trailer tone and an inter-record gap (a blank spot).

When an external program is calling cassette functions via the jump locations, the sync bytes and the leader and trailer tones with an inter-record gap are generated by the SCI. The header and data information are the responsibility of the calling program.

Monitor Commands

The SCI monitor will accept both upper and lower case characters. In the command mode, bit 7 is ignored.

In the following explanations, CR means Carriage Return, or simply Return. ADDR means a one to four character hex address. Commands, their operands, and hex addresses must be separated by one space.

AI K, P, or S(CR) — Assign Input device, either Serial, Parallel, or the Keyboard port at IC-44. When reset is activated, input returns to the device specified by the DIP switch (see page 11).

AO P, S, or V(CR) — Assign Output device, either Parallel, Serial, or Video interface using the SCI video software driver.

D ADDR(CR) — Dump hex data from memory. Dumps one line of 16 hex bytes, starting at ADDR. To dump additional data, hit the space bar. To return to the command mode, hit any other character.

DA ADDR ADDR(CR) — Dump ASCII; displays memory data in hex bytes, and the ASCII equivalent. Useful for locating tables and comments in programs.

E ADDR(CR) — Enter memory. The memory address and its content are displayed. If a new byte is desired, type it in and it will be entered into memory. The byte actually stored will be displayed, and the next memory location will be displayed. If the content is to remain unchanged, typing a space will bring the next byte. Typing a non-hex character will terminate the routine. If you want to move backward in memory, hit Control H, a backspace.

EM ADDR(CR) — Enter Memory. Similar to the E command, but no data is read from memory. Sixteen bytes may be entered per line of type. This routine saves paper when using a printer for console output. Use the DA or D command to verify correct entry of the data into memory.

G ADDR(CR) — Go. Transfers execution to that address.

H ADDR ADDR(CR) — Hex arithmetic. Calculates the sum and difference of the two hex numbers. The first number printed is the sum, the second is the result of subtracting the first number from the second.

I NN(CR) — Input from port NN. The byte at the specified port is displayed. To repeat the input, hit the space bar. To return to the monitor, hit any other key.

M ADDR ADDR ADDR(CR) — Move memory from the block specified by

M ADDR ADDR ADDR(CR) — the first two addresses, to a block starting at the third. The data is moved and then verified. Any errors that occurred in the move are listed. Can be used as a simple memory check, see appendix G.

O NN MM(CR) — Output the hex byte MM to the port NN. To repeat the function, type a space. To return to the monitor, hit any other key.

P ADDR ADDR(CR) — Program a 2708 with data from memory beginning at the first address, to the 2708 at the second address, which for the SCI is H8ØØ (D8ØØ, E8ØØ, etc). When the 2708 is programmed according to Intel specifications, the data is checked, and any errors listed. Allow about 2 1/2 minutes for execution.

RC(CR) — Read Cassette. Reads a cassette tape of the format specified earlier. When finished, writes COMPLETE. If the checksum read in doesn't agree with the checksum on the tape, an error has occurred. In this case, the monitor writes TAPE ERROR.

RS ADDR ADDR(CR) — Read Specify. If no address is given, reads all information in the file and places it in memory, including the header, beginning at ØØØØ. If one address is given, the information is placed in memory starting at that address. If two addresses are given, that block of memory is filled with the first part of the file. The recorder is stopped when it reaches an inter-record gap. The checksum is calculated to check for errors, except where two addresses are given. In that case, TAPE ERROR always appears.

RV(CR) — Read Verify. Reads a file and compares it with memory. Useful for checking files as they are written to make sure there are no errors.

S ADDR ADDR N1 N2..N9 — Search the memory block specified by the two addresses, for the hex character string N1 N2...N9. The address of the start of each string found is printed. Up to 9 bytes may be specified, and a minimum of one, or the routine will loop forever. If all memory is searched, allow 50 seconds for execution.

SR NNNN(CR) Set Read speed for the cassette. The appropriate hex number, NNNN, is given in the Baud Rate table, page C-1. When reset is hit, the SCI returns to the read speed specified in the initialization routine.

SS NNNN(CR) Set Serial speed for the serial port. Same requirements as SR.

SW NNNN(CR) Set Write speed for the cassette. The requirements are the same as for SR.

V ADDR ADDR ADDR(CR) Verify a block of memory specified by the first two addresses, with a block of memory starting at the third address. Useful for checking the programming of 2708's, or changing bits in different memory blocks.

WC ADDR ADDR(CR) Write Cassette, the memory block specified by the two addresses, in the format defined earlier. The routine says WRITTEN when done. Automatically starts and stops the recorder as do all tape commands.

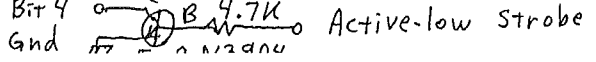
Z ADDR ADDR NN(CR) Zero memory from ADDR to ADDR. If NN is not given, zeroes are written. If NN is given, the memory block is filled with that hex byte. Makes a simple means to fill memory with sync bytes to write a sync tape for recorder set-up. Or fill memory with FF to check the erasure of 2708's.

Hitting Escape will cause an exit from all routines, and return to the command mode. If used during a cassette routine, reset must be hit before trying to use the cassette routine again, or Go to the start of the monitor (H000), or output 00 to port H2 the cassette port control.

Cassette commands turn the relays on and off to control two recorders, one for read and one for write. If only one recorder is used, wire the two sets of relay contacts together in parallel, as outlined on page 6, Cassette Control.

Keyboard problems

Keyboards with unlatched outputs may have problems with Escape functions. Increasing the keyboard strobe pulse to 20 ms will allow the strobe and escape character to be recognized, while the monitor is executing a program. Also, some encoders are noisy on the data lines when not active. A false escape character may be occasionally generated which the SCI monitor will interpret as a legitimate escape. Connecting a transistor such as a 2N3904 to bit 4 of the keyboard data lines, and driving it with an active-low strobe will eliminate the problem.



Using the 8253 for a sweep generator.

Using the cassette output pin (2 of IC pad 41 for low level, and pin 3 for high level) as the signal source, and the following program, the 8253 can be programmed to sweep any range of frequencies. This range can start as low as 30 hz, and go as high as 1 mhz (to use the 1 mhz band, the output capacitors of the cassette system must be bypassed, so get the signal direct from pin 11 of IC-31, the 74LS386).

The program as written produces an electronic siren, which provides interesting results when piped through a stereo. For a slowly changing tone that can be used to check the response of an audio amplifier, change the following lines:

```
0000 21 00 30  this changes the start frequency
000A 1E 80     this changes the total range
0013 01 00 E0  this changes the magnitude of the step
```

Program to sweep the 8253

```
0000 21 00 0C  set the starting frequency to 651 hz
0003 01 A0 FF  set B to subtract 60hex each freq change
0006 3E 76     set up 8253
0008 D3 DB     SCI address set for D000. change to suit
000A 1E 10     set number of steps
000C 7D        output L to 8253 counter
000D D3 D9     change D9 for other address of SCI
000F 7C        output H to 8253 counter
0010 D3 D9     change D9 for other address of SCI
0012 C5        Push B to save
0013 01 00 FA  set up a delay
0016 03        increment BC
0017 78        MOV A,B
0018 B1        ORA C     all zeroes yet?
0019 C2 16 00  JNZ       if not, loop
001C C1        POP B     restore BC
001D 09        DAD B     add B to HL
001E 1D        DCR C     decrement step counter
001F C2 0C 00  JNZ       loop until done
0022 C3 00 00  JMP       start all over
```

Try other variations of locations 0000, 000A, and 0013 for different sound effects.

Simple Memory Checker

Using the E command and the M command, a simple check of a block of memory can be made to look for hard errors (Always bad bits). This is a simple, fast memory check. Since it only executes once, it is not always able to find elusive errors, but will pinpoint hard memory failure.

Using the E command, to check and verify entry, enter the following sixteen bytes of data in the first sixteen locations of the block of memory to be tested:
ØØ 11 22 33 44 55 66 77 88 99 AA BB CC DD EE FF

Hit return and using the Move command, enter:

M ADDR1 ADDR2 ADDR3(CR)

ADDR1 is the beginning address of the sixteen bytes of data, ADDR2 is the ending address of the block of memory, minus 16, and ADDR3 is ADDR1 plus 16.

Example:

A block of unknown memory at 2ØØØ hex to 2FFF is to be tested. First, enter the sixteen test bytes:

E 2ØØØ(CR)
2ØØØ NN ØØ ØØ
2ØØ1 NN 11 11
2ØØ2 NN and so on until all 16 bytes are correctly entered. NN above is the present content of the memory location.

Then use the Move command :

M 2ØØØ 2FEF 2Ø1Ø(CR)

This command then fills the block of memory with the sixteen bytes of test data and checks for any errors. If any errors do show up, the memory is unusable and should be tested thoroughly to locate the problems.

Interfacing the SCI Monitor to ESP-1

ESP-1 is an Assembler, Editor, and Monitor for an 8080, written for the 8080 by Michael Shrayer. The following patches are for the SCI Monitor version 1.5.

Location	Code before	for SCI	
6C52		CD Ø6 HØ	Output
6CAD		CD Ø6 HØ	Output
7ØC6	DB ØØ	C3 1E	Input
7ØC8	E6 Ø2	HO	
7ØCA	CA C6 7Ø		
7ØCD	DB Ø1	C3 B7 H3	Escape Routine (1.5)
7ØCF	E6 7F		
7ØD1	C9		
7ØDF	DB ØØ	ØØ ØØ	Output
7ØE1	E6 Ø1	ØØ ØØ	"
7ØE3	CA DF 7Ø	ØØ ØØ ØØ	"
7ØE6	78	78	"
7ØE7	D3 Ø1	C3 Ø6 HØ	"
7ØE9	C9		
77E8	26	29	Cassette Read
77EC	26	29	" "
77FØ	26	29	" "
77FA	26	29	" "
7815	26	29	" "
781D	CD ED 7Ø	CD ØC HØ	" "
782Ø	21 ØØ 6Ø	CD ED 7Ø	" "
7823	C3 DE 73	21 ØØ 6Ø	" "
7826	CD BD 7Ø	C3 DE 73	" "
7829	DB 6E	CD BD	" "
782B	E6 1Ø	7Ø C3	" "
782D	C2 26 78	Ø9 HØ 78	" "
776C	CD A7 77	C3 74 77	Cassette Write
7776	A7	AA	" "
777A	A7	AA	" "
777E	A7	AA	" "
7782	A7	AA	" "
7780	A7	AA	" "
779A	A7	AA	" "
77A1	21 5F 78	CD 12 HØ	" "
77A4	C3 E5 76	21 5F 78	" "
77A7	F5	C3	" "
77A8	CD BD 7Ø	E5 76 F5	" "
77AB	DB 6E	CD BD	" "
77AD	E6 2Ø	70 F1	" "
77AF	C2 A8 77	C3 ØF HØ	" "

In the Escape routine, if ESC is typed the SCI monitor will take over. This is not a standard character for ESP-1.

In the cassette read routine, if ESP-1 detects an error, the SCI monitor must be reset to turn off the recorder, and reset the cassette port.

The write cassette routine takes full advantage of the SCI monitor to write a tape and control the recorder.

In the above, H stands for the 4k memory block of the SCI (DØ, EØ, etc.).