OHIO SCIENTIFIC

SALES/TECHNICAL

NEWSLETTER # 22

November 9, 1979

OS-CP/M UPDATES

All OS-CP/M updates are to be handled by LIFEBOAT. <u>Only original</u> diskettes can be updated. The list below details the actual updates. The ESCORT diskette will be updated if included with a COBOL or FORTRAN update. New OS-CP/M from the factory includes the original (old) manuals only, with addenda sheets. See Sales Notes #1 for update procedure.

<u>COBOL Update</u>

PRICE $25.00 + $25.00 for manual

Includes:

COBOL V 3.3T
BASIC 4.5T
Z-80/8080 MACRO ASSEMBLER
ED
LIBRARY MANAGER
PIP
DDT
STAT
SYSGEN
LINKING LOADER
SUBMIT
DUMP
ZBIOS
CA-1QX DRIVER
NEW 6502 DISC DRIVERS (FLOPPY A,B,C,D,)
NEW COBOL MANUAL

LIFEBOAT now offers a service for converting IBM format diskettes to OS-CP/M Format and visa versa. Original diskettes or proof of purchase must be provided with the diskettes. Please make sure that the destination diskettes contain sufficient room for the programs to be transferred to them. Technical over views for any of LIFEBOATS software advertised are free from LIFEBOAT. Please contact LIFEBOAT for details.

FORTRAN Update

PRICE $25.00

Includes:

FORTRAN V 3.30
BASIC V 4.51
Z-80/8080 MACRO ASSEMBLER
ED
8080 ASSEMBLER
LIBRARY MANAGER
LINKING LOADER
DDT
PIP
SUBMIT
STAT
SYSGEN
LOAD
DUMP
LPTDRV
DSKDRV
ZBIOS
IOINIT
INIT
LUNTB
CA-10X DRIVER
NEW 6502 DISK DRIVERS (FLOPPY A,B,C,D)

ATTENTION DEALERS

C2-8P DF, C2-8S DF, and CD-2 units are now being shipped with the Floppy case
cover separately boxed. The new CD-2 drives weigh slightly over 50 pounds.
Since 50 pounds is the weight limit of UPS the cover is being boxed with the
manuals and software. This allows us to continue shipping via UPS.

RETROACTIVE FIX - CD-23 ONLY

The CD-23 fix shown on page 5 of Techletter #11 concerning "seek timeouts"
also corrects "status error" (i.e. error 13 under LEVEL III).

NEW OS-65U UTILITIES

The following changes, additions have been made to OS-65U as of 11/9/79:

1) RSEQ - resequence utility

2) NECDRV - NEC driver utility

3) EDITOR - line oriented editor

4) / - utility to select EDITOR or RSEQ

5) INSWAP - program containing SWAP command

6) FILLER - program containing PACK FIELD command

7) MACCMD - contains SWAP and PACK FIELD

SHTEST / OKTEST

CAUTION: SHTEST AND OKTEST are disc test programs under OS-65U. These programs are destructive programs. ANY area of the disc over which these programs are RUN WILL BE ERASED. In other words any data in that area over which SHTEST or OKTEST is RUN WILL BE DESTROYED.

2MHz UPDATES

Conversion of C3-Systems to 2MHz 6502, 6800 operation and 4MHz Z80 operation.

Modifications are required to the backplane board, 580 or 581, 510 board, and 520 boards. In addition, wait diodes must be installed on the peripheral boards in the system. Also a wait switch and LED indicator should be installed so that 1MHz or 2MHz operation can be indicated.

For C3-S1 and C3-OEM systems, modify the 580 backplane board as shown in Figure 1. The addition of four (4) 470 resistors is for addresses A16-A19. In addition, install a wire as shown in detail 1 to the front panel switch and LED indicator as shown in Figure 2. Mounting of the speed switch and LED for C3-OEM's is shown in Figure 3. Wiring is shown for C3-S1 machines in Figure 4. Mounting of the speed switch and LED for C3-S1's is shown in Figure 5. Also, the +5 volt and ground wire for the switch and LED should originate from the backplane power bus.

For C3-A based computers the changes shown in Figure 6 should be made on the 581 backplane board. The wiring to the front panel speed switch and LED is the same as the 580 board used in C3-OEM's. The locations of the speed switch and mounting of the LED is shown in Figure 7.
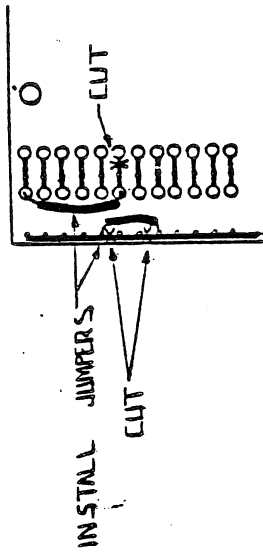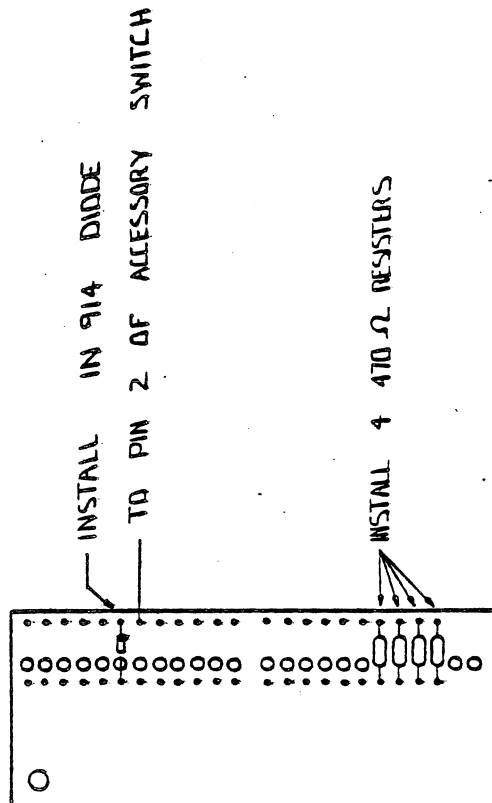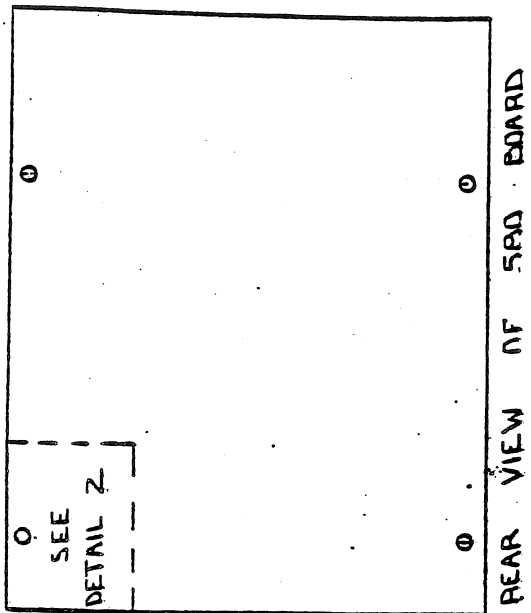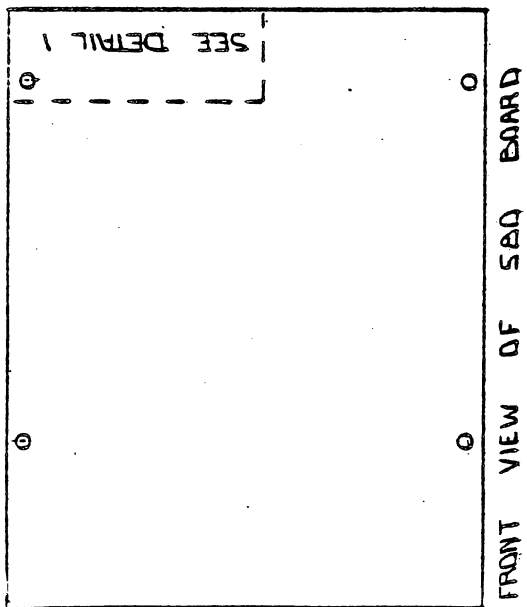
The following modifications are common to both C3-OEM, C3-S1 and C3-A computers.

The changes to the 510 board are shown in Figure 8. These changes are shown on the 510 schematics enclosed dated October 29, 1979.

On the 520 boards in the system make the changes as shown in Figure 9.

In addition, all other boards in the system not designed for 2MHz operation should have wait diodes installed on them.

The following RAM chips should operate at 2MHZ : SEMI 4200B, 2114 RAM chips good for 300 nanoseconds. Note that N-MHZ software is required to run at N-MHZ. N-MHZ OS-65U is standard as of 11/9/79. 2MHZ C3's become standard as of 10/29/79.
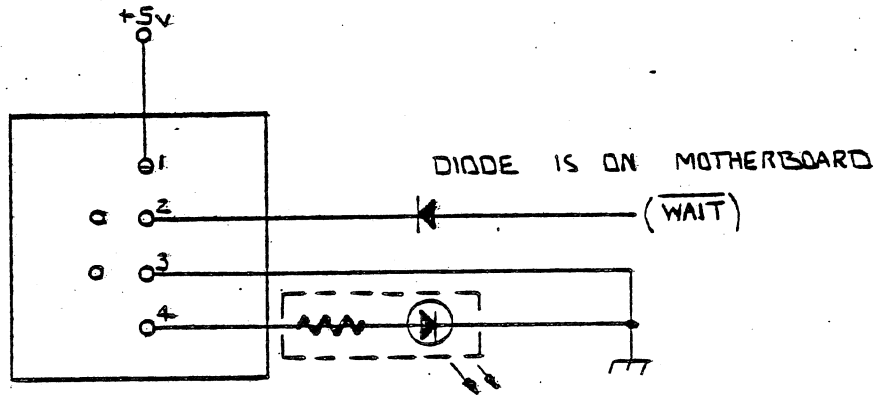
REAR VIEW OF SBD BOARD

SEE
DETAIL 2

FRONT VIEW OF SBD BOARD

SEE DETAIL 1

CUT

INSTALL JUMPERS

CUT

DETAIL 2

INSTALL IN 914 DIODE
TO PIN 2 OF ACCESSORY SWITCH

INSTALL 4 470 Ω RESISTORS

DETAIL 1

FIGURE 1

OSI PART # L-LED-2

DIALITE PART # 507-4757-3331-500

DIODE IS ON MOTHERBOARD

DIODE IS ON MOTHERBOARD
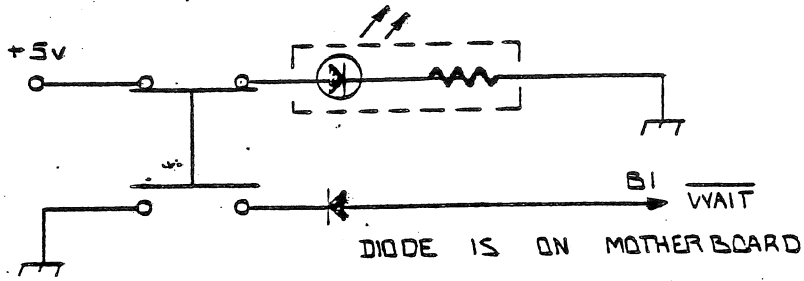
REAR VIEW OF ACCESSORY SWITCH

FIGURE 2

SPEED SWITCH

INSTALL QSI PART # L-LED-Z

$\frac{9}{32}$" DIA.

2.25"

1.15"

FIGURE 3

SPEED SWITCH
DSI PART # T02
CUTLER HAMNER PART # JBT-103
ARROW HART PART # CTS-3
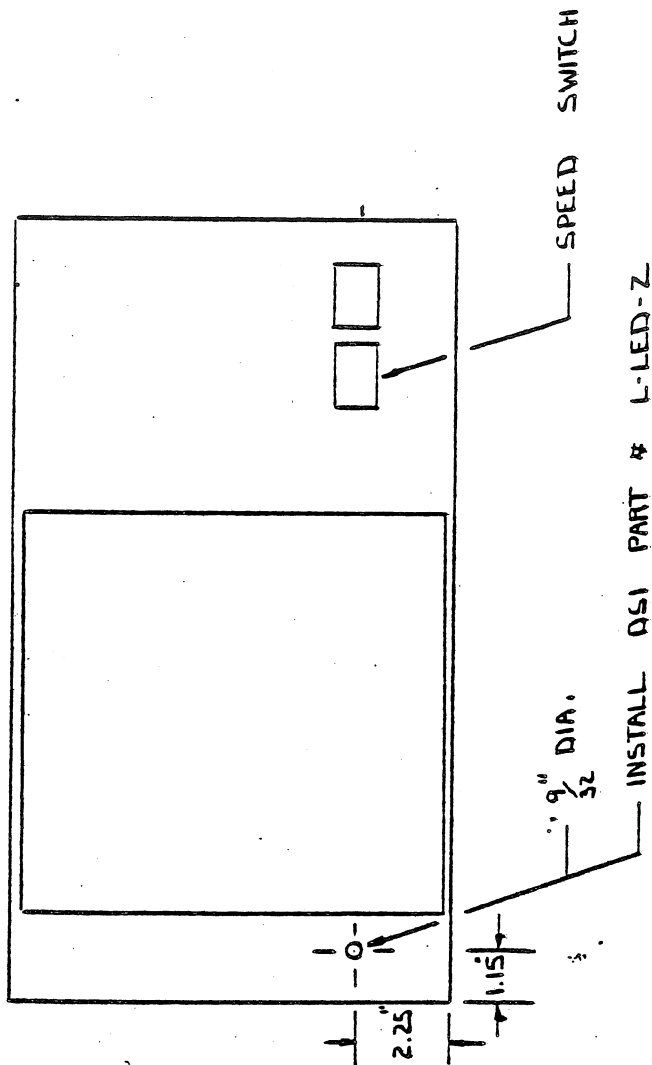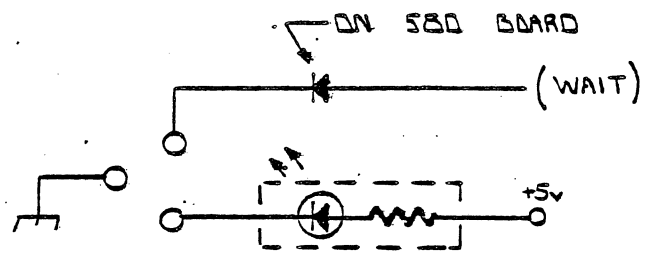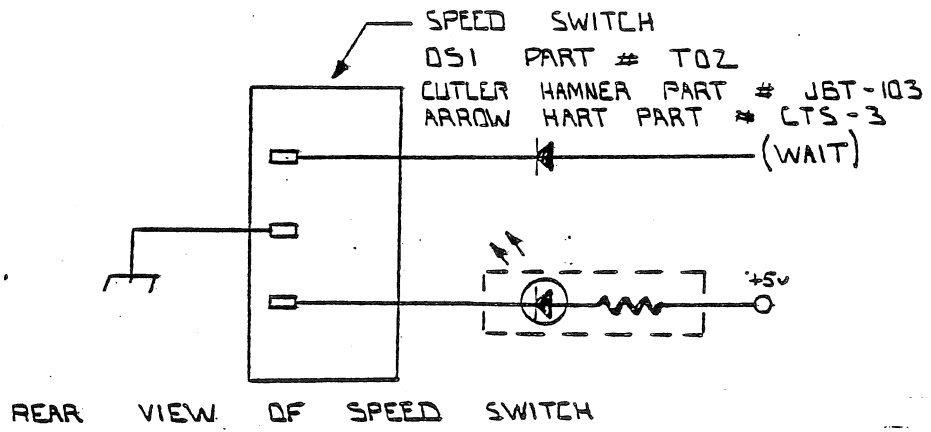
(WAIT)

+5v

REAR VIEW OF SPEED SWITCH

ON S80 BOARD

(WAIT)

+5v

DSI PART # L-LED-2
DIALITE PART # 507-4757-3331-500

FIGURE 4

2.25"

|1.15"|

$\frac{9}{32}$" DIA.

INSTALL OSI PART # L-LED-2

INSTALL SPEED SWITC
OSI PART # TO2

INSTALL SPEED SWITCH
OSI PART # TO2

FIGURE 5

#22, 10

OSI S81

SEE DETAIL 1

SEE DETAIL 2
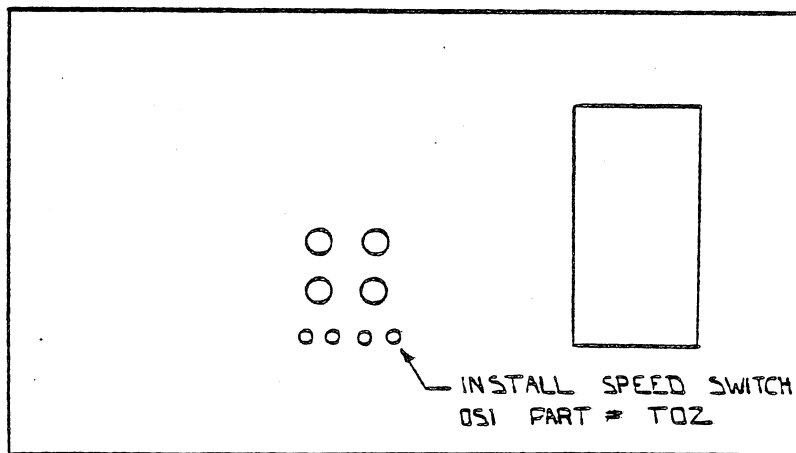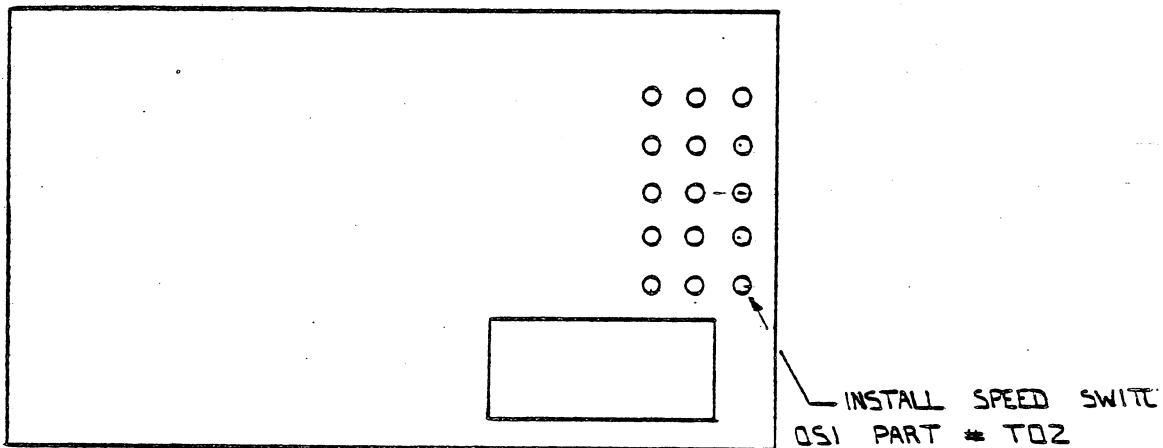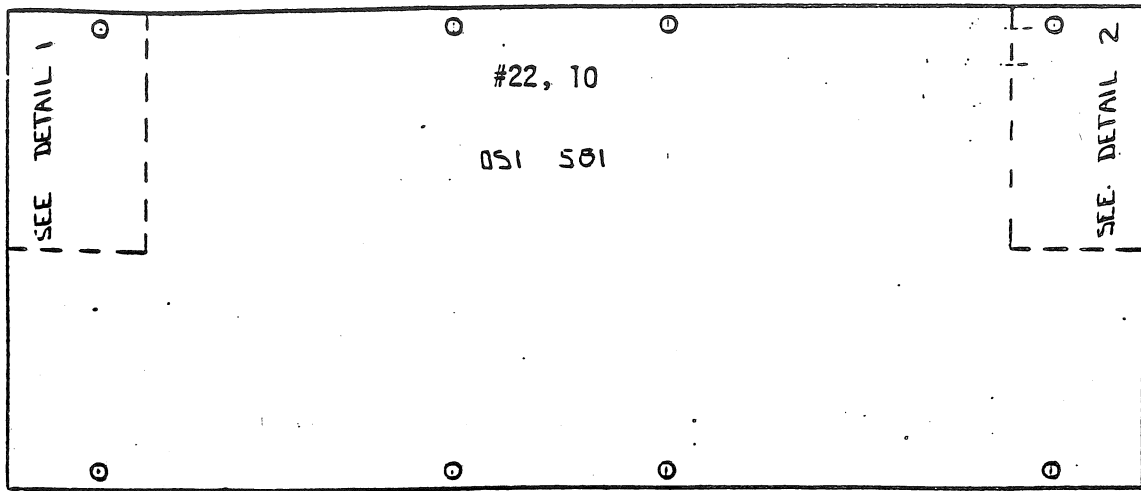
FRONT VIEW OF S81 BOARD

INSTALL 4 470Ω RESISTERS

INSTALL 4 470Ω RESISTERS

DETAIL 1

INSTALL IN 914 DIODE

ADD JUMPERS

CUT

CUT

TO PIN 2 OF ACCESSORY SWITCH

INSTALL 4 470Ω RESISTERS

DETAIL 3

DETAIL 2

SEE DETAIL 3
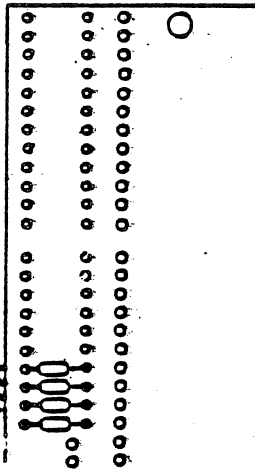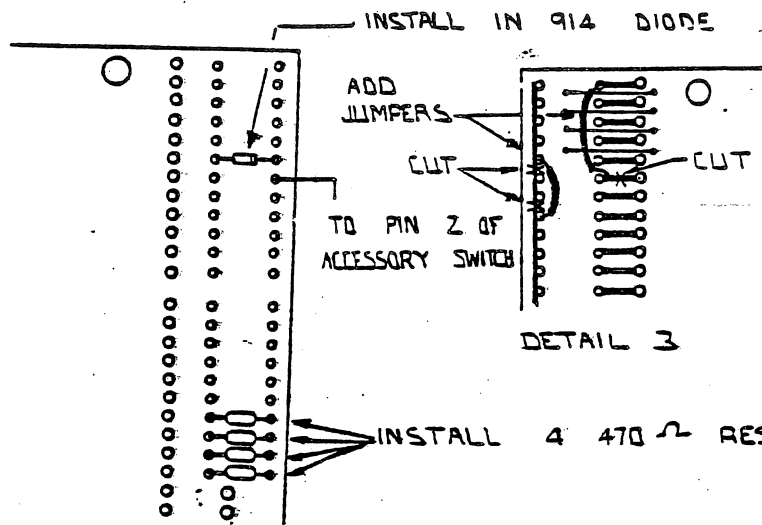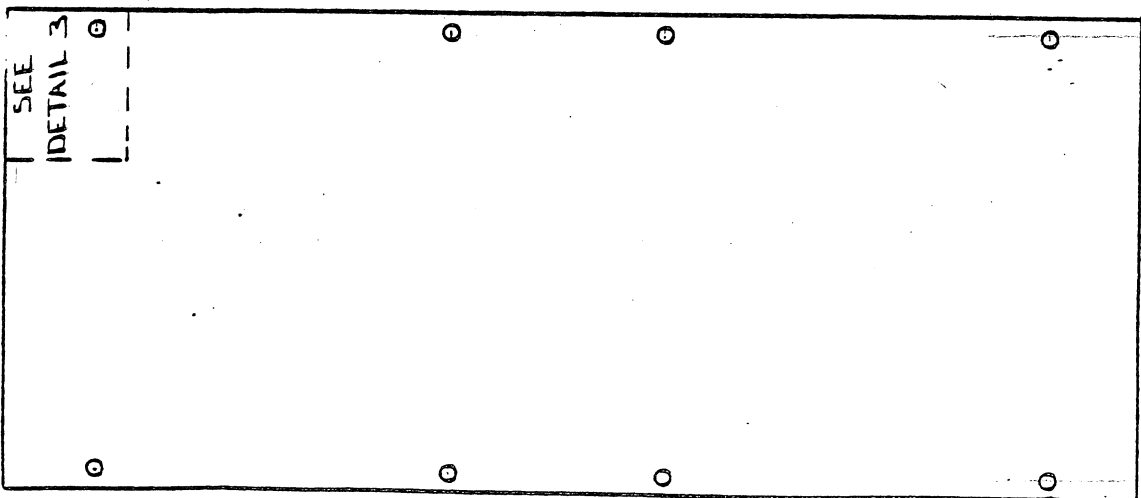
REAR VIEW OF S81 BOARD

FIGURE 6
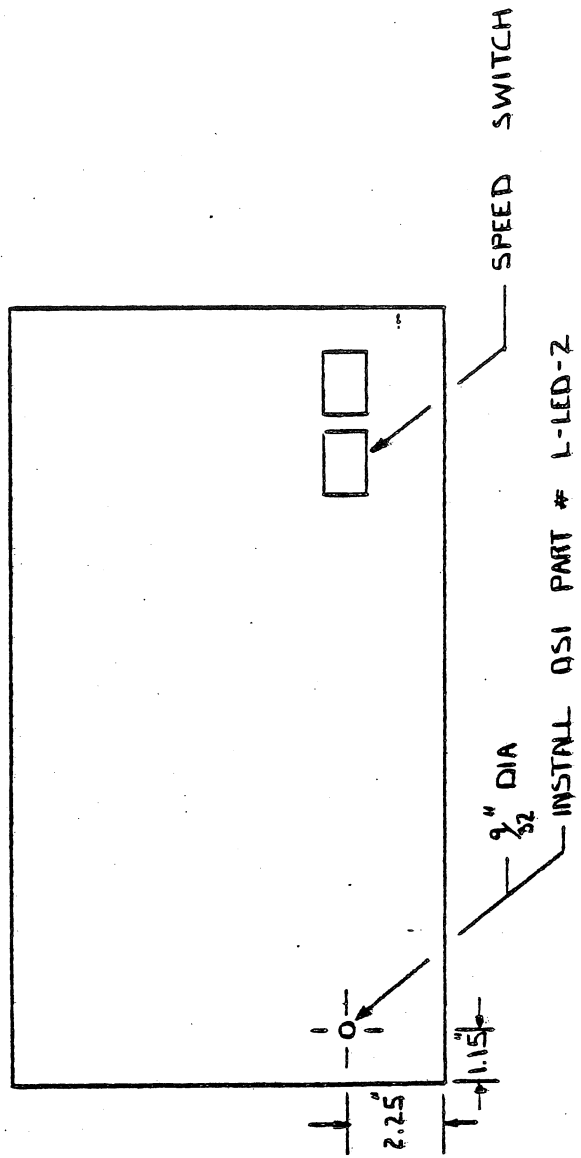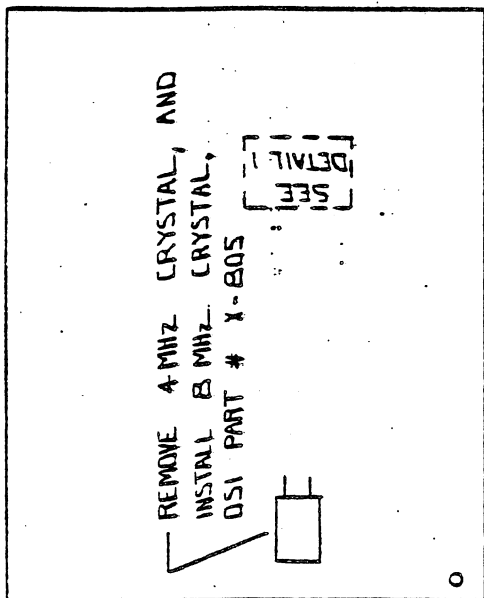
SPEED SWITCH

INSTALL QSI PART # L-LED-2

$\frac{9}{32}"$ DIA

2.25"

1.15"

FIGURE 7

REAR VIEW OF SIO REV C

SEE DETAIL 2

FRONT VIEW OF SIO REV C

REMOVE 4 MHz CRYSTAL, AND
INSTALL 8 MHz CRYSTAL,
OSI PART # X-805

SEE DETAIL 1

INSTALL JUMPER

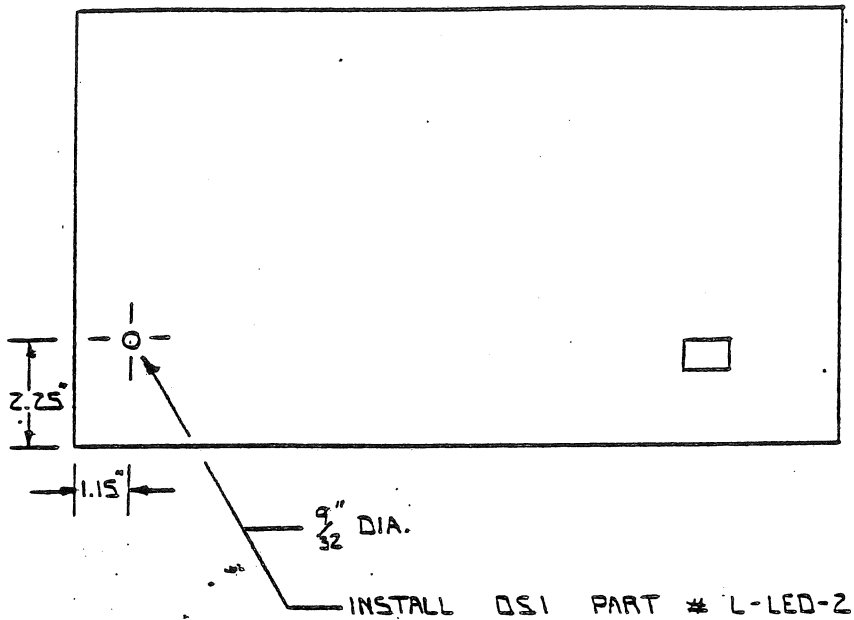THIS CUT IS ALREADY ON BOARD

REMOVE JUMPER

INSTALL JUMPERS

INSTALL

U31

U32

U33

U34

U35

U36

U37

U38

U28

U23

U24

UT

DETAIL 2

U39

8T95

INSTALL IN 914 DIODE

DETAIL 1

FIGURE 8

SEE DETAIL 2
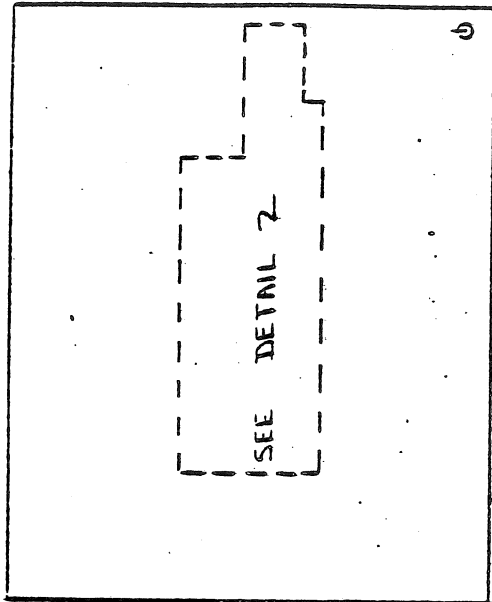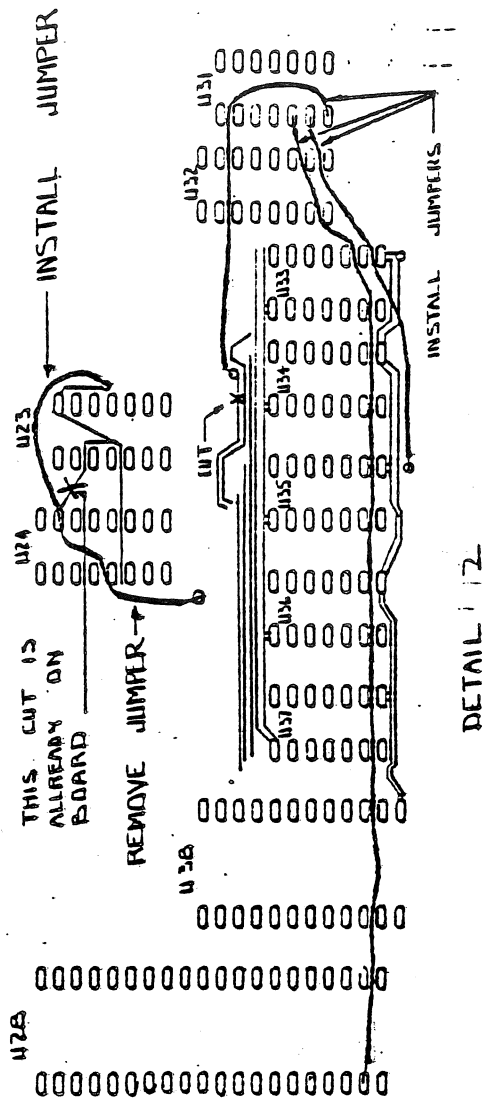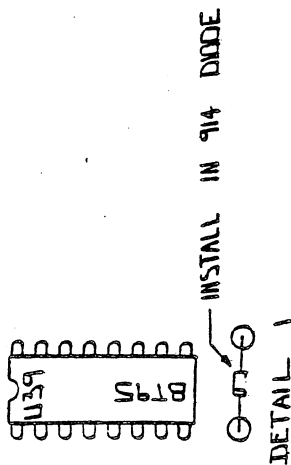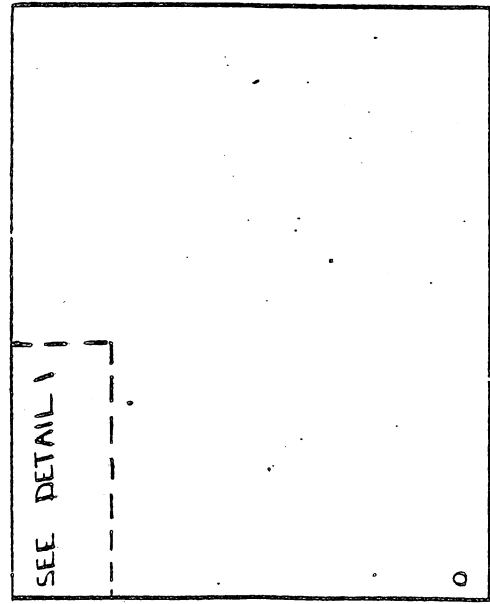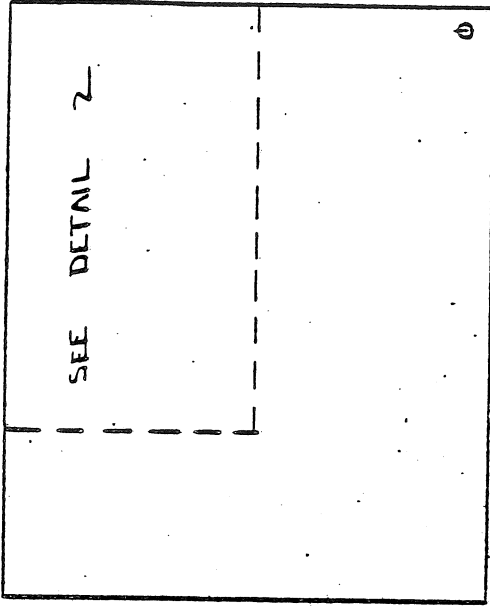
REAR VIEW OF 520 REV B

#22, 13
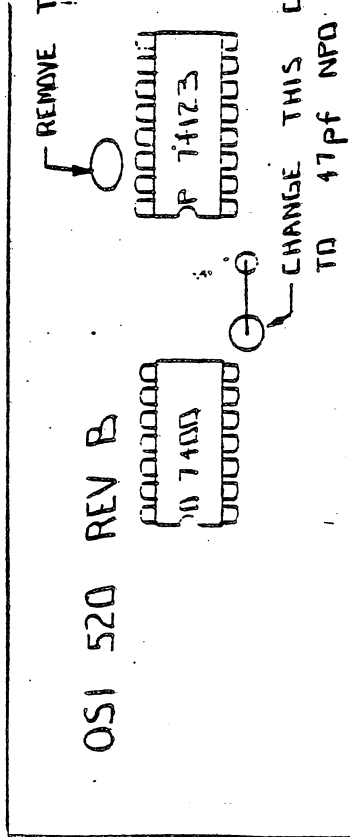
INSTALL 8 .1µf 16 WVDC BYPASS CAPACITORS
BETWEEN VDD AND GROUND

DETAIL 2

SEE DETAIL 1

FRONT VIEW OF 520 REV B

OSI 520 REV B

REMOVE THIS CAPACITOR

P 74123

74LS00

CHANGE THIS CAPACITOR
TO 47pf NPO

DETAIL 1

FIGURE 9

8T95 TYP

($\overline{CWR}$) — 18 U48 9 — (R/W) B4Ø → R/W

(CLK) — 2 U48 3 — (Ø2) B39 → Ø2

(RFSH$_c$) — 2 U34 12 — 11 U4 1Ø — 1Ø U39 9 — (Ø2·VMA) B42 → Ø2·VMA

(MREØ$_c$) — 1 U33 2 — 1,13

($\overline{W R}$) — 1Ø
($\overline{R D}$) — 9 U31 8

6 U39 7 — (VMA) B41 → VMA

(PS$_c$)

+5v

R3 1KΩ   R4 1KΩ

(CLK) — 11 Ø2 U6 13 — 9 Ø2 U6 1Ø — 5 Ø2 U6 4 — 13 ØØ U23 11 — 9 U4 8

12   8   6   12

(Ø1$_B$)

(VMA$_B$)

(Ø2$_B$)

12 U18 11 — (Ø2·VMA)

2 U18 3 — (Ø2)

(IDD) — 13 ØØ U53 11 — 13 U4 12 — (BE$_B$)

U52

12

4 U4 3 — U43

($\overline{IDD}$) — 9 ØØ U53 8 — ($\overline{RE_B}$)

4 U18 5 — (VMA)

($\overline{PS_B}$)

OHIO SCIENTIFIC

product name/number
MODEL 51Ø REV C

date	revision	page	status	sheet 4 of 11
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DRAWN~ J.L.K.				

8T95 TYP (PSc)

A11
A13
A5
A4
A7
A9
A18
A14
A6
A15
A8
A12
A8
A2
A1
A3

D5
D1
D7
D3

D4
D2
DØ
D6

U26 U27 U39 U40 U29 U30 U28 Z-80 U43 U44 U52 U48

(RDY) RDY (RFSHc) (WR) (MREQc) (INMI) (IIRQ) (RES) (RD) (CLK) (PSc) NOT USED (PSc) DD (DD) (IDD) NOT USED

+5v

R26 220Ω R25 R6

WAIT VCC BREQ RFSH WR MREQ NMI IRQ RES RD D6 D0 D2 D4 D3 D7 D1 D5

	OHIO SCIENTIFIC	product name/number
		MODEL 510 REV C
		Z-80 CIRCUITRY

date	revision	page	status	sheet 5 of 11
29 OCT 1979 DRAWN ~ J.L.K.				

SYSTEM CLOCK SPEED CHART AT 4 MHz

CUT HERE FOR 4MHz XTAL

X1 (8.000 MHz)

470Ω R22   470Ω R23   2.2KΩ R32   +5v

C9 27pf

U31   U31   U31

ADD JUMPER FOR 4MHz

	WAIT	NORM
6502	.5	1
6800	.5	1
Z-80	1	2

(HSCK 1)

U14 7473

U23   U23   U23

U33 04

U33 04   U34

(PSc)

U19 04   R5 +5v NOT USED

WAIT B1   (WAIT)

U5 7476   U5 7476   (CLK)

(110 BAUD)

U22

1 INB	D 11	75 BAUD
14 INA	C 8	150 BAUD
2 RD1	B 9	300 BAUD
3 RD2	A 12	600 BAUD

7494

R32 +5v 2.2KΩ

U24 74163

U33 04   U54 04   U25 20

R24 2.2KΩ +5v C14 220pf

U32 74123

U21 7494

1 INB	D 11	1200 BAUD
14 INA	C 8	2400 BAUD (Rx CLK)
2 RD1	B 9	(Tx CLK) 4800 BAUD
3 RD2	A 12	9600 BAUD

19.2 K BAUD

SYSTEM CLOCK SPEED CHART AT 8 MHz

	SLOW OR WAIT	FAST
6502	1 MHz	2 MHz
6800	1 MHz	2 MHz
Z-80	2 MHz	4 MHz

OHIO SCIENTIFIC

product name/number
MODEL ~ 510 REV C
SYSTEM CLOCK AND BAUD RATE GEN.

date	revision	page	status	sheet 9 of 11
29 OCT 1979 DRAWN ~ J.L.K.				

Z-80 MEMORY ACCESS MOD

Cut Here

Add Jumper

From
RFSHC

From
MREQC

WR From
Z-80
PIN 22

RD From Z-80, PIN 21

1

04
U33

2

10
U34

12

To U33, PIN 11

To U39, PIN 6

10

00
U31

8

9
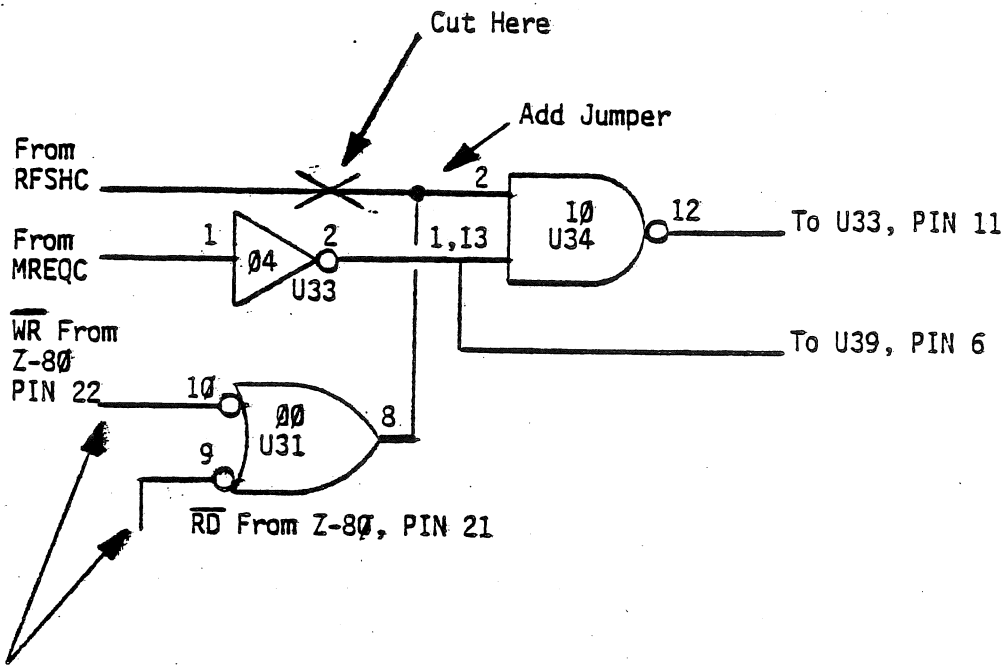
Add Jumpers

(See Sheet 4 of 11, 510 Rev C Schematic)

The SEMI 4200 RAM chips used on the 520 Static RAM boards are psuedo-Static
Chips. These chips require a certain amount of "set up" time between accesses.
They also require that the R/W line be defined before they are enabled. The
original R/W circuitry could access memory in such a way that some 4200 chips
would operate unreliably. This was due to the R/W line transition from READ to
WRITE occurring as the chip was being enabled. The change shown prevents the
4200's from being enabled until the R/W line has stabilized.

Systems shipped after 10/31/79 have the above modification installed.
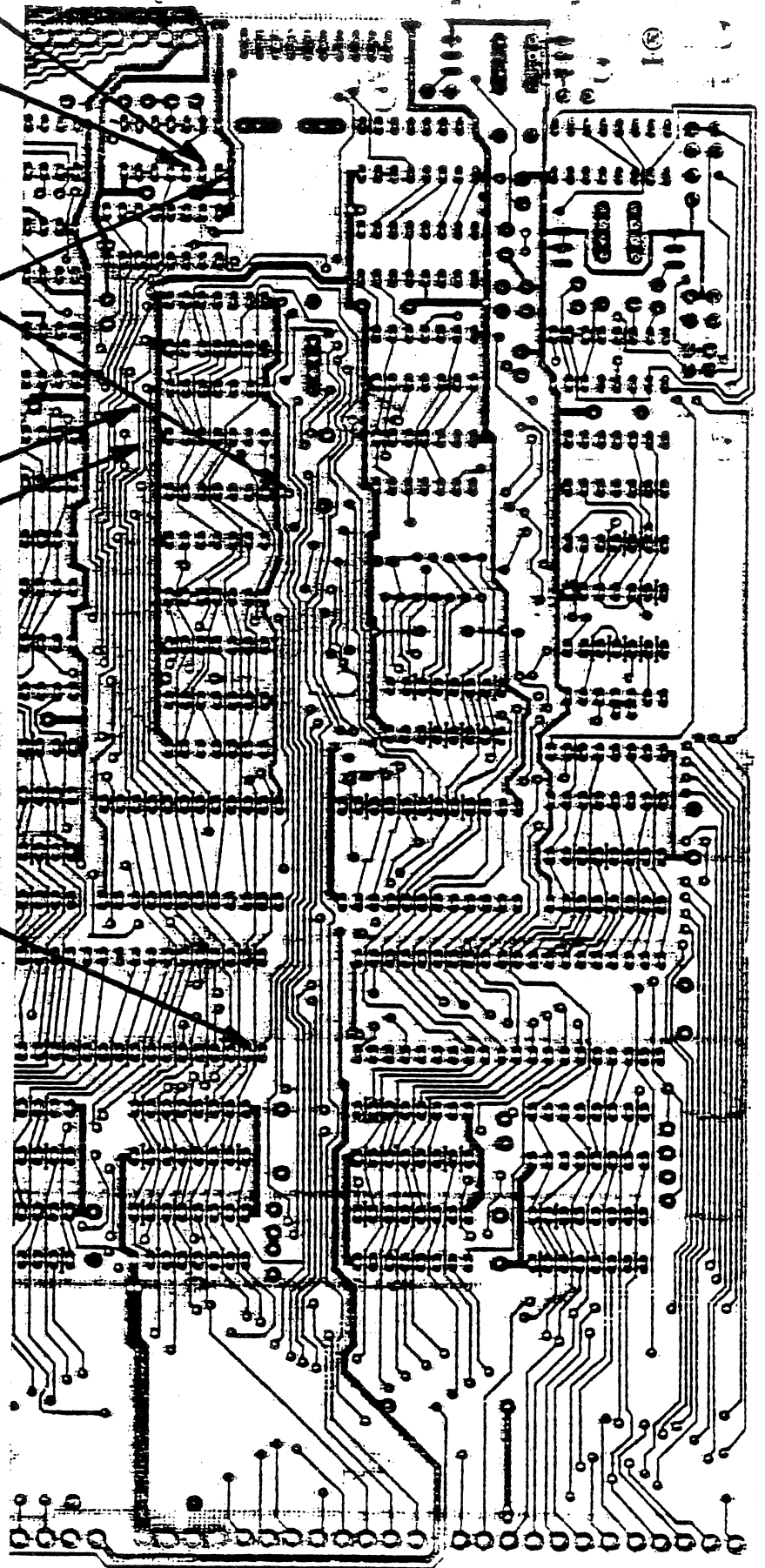
#22, 18

REAR VIEW OF 510 REV C

Z-80 CHANGE

CUT HERE

ADD JUMPER FROM PIN #9
OF IC-U31 TO PIN #21 OF
THE Z-80 (U28)

ADD JUMPER FROM PIN #8 OF
IC-U31 TO PIN #2 OF IC-U34

ADD JUMPER FROM PIN #10
OF IC-U31 TO PIN #22 OF
THE Z-80 (U28)

505 REVISION B

The 505 Revision B board in the C4P MF and C8P DF accommodates both a modem and printer. Baud rate and handshaking may be configured in several ways. The factory configuration provides software selection of printer or modem as well as two baud rates. The table below shows the POKES for the factory configuration.

```
POKE   63235,52    Selects Modem
POKE   63235,60    Selects Printer

POKE   64512,1     Selects 1200 Baud
POKE   64512,2   · Selects  300 Baud
```

CTS/CTSM - High true input indicating printer or modem "Ready" (TTL or RS-232)

RTS -   - High true output indicating CPU "Ready" (TTL)

DCD   - High true input from modem indicating "Data carrier detected" (TTL or RS-232)

U6B and U6C on the 505 Revision provides clock signals for the serial interface. The outputs are listed in the following table.

```
9600 BAUD    (Actual 16 x 9600)    PIN # 12,   IC-U6B
4800 BAUD    (Actual 16 x 4800)    PIN #  9    IC-U6B
2400 BAUD    (Actual 16 x 2400)    PIN #  8    IC-U6B
1200 BAUD    (Actual 16 x 1200)    PIN # 11    IC-U6B
 600 BAUD    (Actual 16 x  600)    PIN # 12    IC-U6C
 300 BAUD    (Actual 16 x  300)    PIN #  9    IC-U6C
 150 BAUD    (Actual 16 x  150)    PIN #  8    IC-U6C
  75 BAUD    (Actual 16 x   75)    PIN # 11    IC-U6C
```

The printer is normally run at 1200 BAUD and the modem is run at 300 BAUD. The BAUD rate is selected by setting the ACIA to divide by 16 for 1200 BAUD and divide by 64 for 300 BAUD.

By changing one connection several other combinations of BAUD rate are possible. The combinations are in the following table. Note that these combinations do not necessarily apply to the printers or modems supplied by Ohio Scientific, Inc.

For all BAUD rate changes cut the foil run between pins #2 and #3 of
IC-U1D and pin #11 of IC-U6B at pin #11 of IC-U6B.

Jumper PINS #2 & #3 of IC-U1D to		BAUD Rate Divided by 16	BAUD Rate Divided by 64	BAUD Rate Divided by 1	
PIN #12,	IC-U6B	9600	2400		
PIN # 9,	IC-U6B	4800	1200		
PIN # 8,	IC-U6B	2400	600		
PIN #11,	IC-U6B	1200	300	19.2K	(Output to
PIN #12,	IC-U6C	600	150		Printer
PIN # 9,	IC-U6C	300	75		Only)
PIN # 8,	IC-U6C	150	37.5		
PIN #11,	IC-U6C	75	18.75		

OS-65U V 1.2 (NMHz) CD-23 FIX 10/29/79

Problem: FD version won't boot if H Disk is on. HD version won't boot at
all.

Applicability: All OS-65U V 1.2 (NMHz) CD-23 versions for which "WAS" applies
(dealer show copies).

RUN"CHANGE","PASS

DISK CHANGE UTILITY

```
MODE: HEX(H), DEC(D) ? H
UNIT ? A
ADDRESS OFFSET ? -2AFD (-2B00 For Hard Disc)
ADDRESS ? 302E
0000302E    3E ? 40
0000302F  4 34 ? /
00003030  C 63 ? 7B
00003031  4 34 ? /
00003032    EF ? 01
00003033  5 35 ? 36
00003034  C 43 ? 4A
00003035  7 37 ? X
```

OK