OHIO SCIENTIFIC TECH NEWLETTER #9

JUNE 22, 1979

SALES NOTES:

THE FOLLOWING BOARDS ARE NO LONGER AVAILABLE:

    CA-6C   430 BARE BOARD
    CA-6S
    CA-7C
    CA-7S

THE CA-6S HAS BEEN REPLACED BY THE ADDITION OF A NEW CONFIGURATION OF
THE CA-10X BOARD. THE CA-101 IS A 550 BOARD POPULATED WITH ONE RS-232
SERIAL PART.

THE 450 AND 455 EPROM BOARDS ARE ALSO NO LONGER AVAILABLE.

CORRECTION TO WP-2 MANUAL - P. 44 - "HOW TO CHANGE DEVICES"

THE CORRECT PROCEDURE FOR CHANGING THE EDIT PRINTER DEVICE NUMBER IS AS
FOLLOWS:

.E X X X⟨CR⟩
A * B A ⟨CR⟩

OSI 9 DIGIT BASIC
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OK
DISK!"CA 3D00=06,1⟨CR⟩
POKE 17920,2∧(N-1)⟨CR⟩
DISK!"SA 06,1=3D00/B⟨CR⟩

WHERE N IS THE DEVICE NUMBER. A REBOOT IS REQUIRED TO MAKE THE CHANGE EFFECTIVE.

WP-2   SECOND RELEASE

THE CONTROL CODES FOR INDIRECT FILES UNDER WP-2 DIFFER FROM THOSE UNDER OS-
65U. THE POKES BELOW MAY BE ENTERED IN THE IMMEDIATE MODE OR MAY BE PLACED
IN BEXEC*. THESE POKES MODIFY OS-65U TO USE THE SAME CONTROL CODES FOR IN-
DIRECT FILES AS WP-2.

POKE 14646,28 : POKE 14677,29
POKE 14684,28 : POKE 14688,29
POKE 14725,28 : REM FOR INDIRECTS

OS-65U POKE TO PERMIT LEADING SPACES ON INPUT


```
10   REM PERMIT LEADING SPACES EXAMPLE
20   REM
30   REM
40   REM THERE CAN BE NO SPACES OUTSIDE OF QUOTES AFTER THE POKE
50   REM UNTIL BASIC IS POKED BACK TO NORMAL!!!!!!!!!!!!!!!!!!!!
60   REM
70   REM
80   REM
90   REM POKE, THEN INPUT, THEN POKE BACK TO NORMAL
100  REM
110  POKE 207,36:INPUT"THIS IS A QUESTION";QA$:POKE207,240
120  REM
130  PRINT: PRINT "QA$ STARTS HERE>";QA$: PRINT: PRINT
140  REM
150  FOR X=1 TO LEN(QA$,X,1)=" " THEN SP=SP+1
160  NEXT
170  REM
180  PRINT "THERE ARE";SP;" LEADING SPACES IN QA$": PRINT
190  REM
200  PRINT "AND THE LENGTH OF QA$ =";LEN(QA$): PRINT
210  REM
220  PRINT "MID$ OF QA$ STARTING AT THE";SP;" CHAR = ";MID$(QA$,SP)
```

OS-65U POKES

POKE TO ELIMINATE OR CHANGE "?" OUTPUT WITH EACH INPUT STATEMENT (i.e. INPUT "TEST"; QA$ PRINTS AS "TEST?").

POKE 2797, ASC ("CHAR DESIRED")

WHENEVER ONE IS WORKING WITH THE DBMSYS THE NEED ARISES TO CLEAR (i.e. PRINT ALL SPACES) FIELD (S). THIS ARISES WHEN ONE IS INITIALIZING THE FILE OR WHEN ONE IS INSERTING BLANK RECORDS, PACKING A FILE, OR DELETING RECORDS AND/OR SPECIFIC FIELDS. THE SPC(X) COMMAND WOULD LEND ITSELF WELL TO THIS EXCEPT THAT A PRINT SPC(X) DOES NOT PRINT A CR AFTER THE SPACES. THE FOLLOWING POKE FORCES A CR AFTER THE SPC(X) FUNCTION. NOTE THAT THIS POKE ALSO FORCES A CR AFTER A TAB(X); STATEMENT.

FOR EXAMPLE:

```
10   FL=10: REM PRIMED FIELD LENGTH (MINUS CR)
20   INDEX <CH> = BODF + OF: REM PNT TO START OF FIELD
30   POKE 2757, 53: REM FORCE CR
40   PRINT SPC (FL) : REM CLR FIELD DO CR
50   POKE 2757, 55 : REM RESTORE TO NORMAL
```

65U V1.1 POKES

MANY PEOPLE HAVE ASKED FOR A METHOD OF ELIMINATING THE   LF ECHOED
AFTER AN INPUT FROM THE CONSOLE. BASIC CALLS A CR/LF SUBROUTINE FROM MANY
PLACES. HOWEVER, ONE MAY POKE TO ELIMINATE THE   LF JUST BEFORE AN INPUT
AND THEN RESTORE THE   LF IMMEDIATELY AFTER THE INPUT.

FOR EXAMPLE:

OS-65U POKE TO ELIMINATE OUTPUT OF LF ON INPUT


```
10   REM DEMO ON ELIMINATION OF LF ON INPUT
20   REM
30   REM
40   REM
50   REM KILL LF ONLY (RETAINS CR)
60   REM
70   POKE 2683,0:  REM POKE LF TO A NULL
80   REM
90   INPUT "THIS IS A TEST",QA$
100  REM

110  PRINT SPC(80) :  PRINT:  REM CLR OFF LINE & DO CR W/O LF
120  REM
130  INPUT"ON THE SAME LINE";QB$
140  REM
150  PRINT SPC(80): PRINT:  REM CLR LINE & DO CR W/O LF
160  REM
170  PRINT "THE FIRST ANSWER WAS ";QA$
180  REM
190  FOR X=1 TO 1000: NEXT:  REM T.D.
200  REM
210  PRINT SPC(80):  PRINT:  REM CLR LINE & DO CR W/O LF
220  REM
230  PRINT "THE 2ND ANSWER WAS ";QB$
240  REM
250  FOR X=1 TO 1000:  NEXT:  REM T.D.
260  REM
270  PRINT SPC(80): PRINT:  REM CLR LINE & DO CR W/O LF
280  REM
290  POKE 2683,10:  REM POKE LF BACK
```
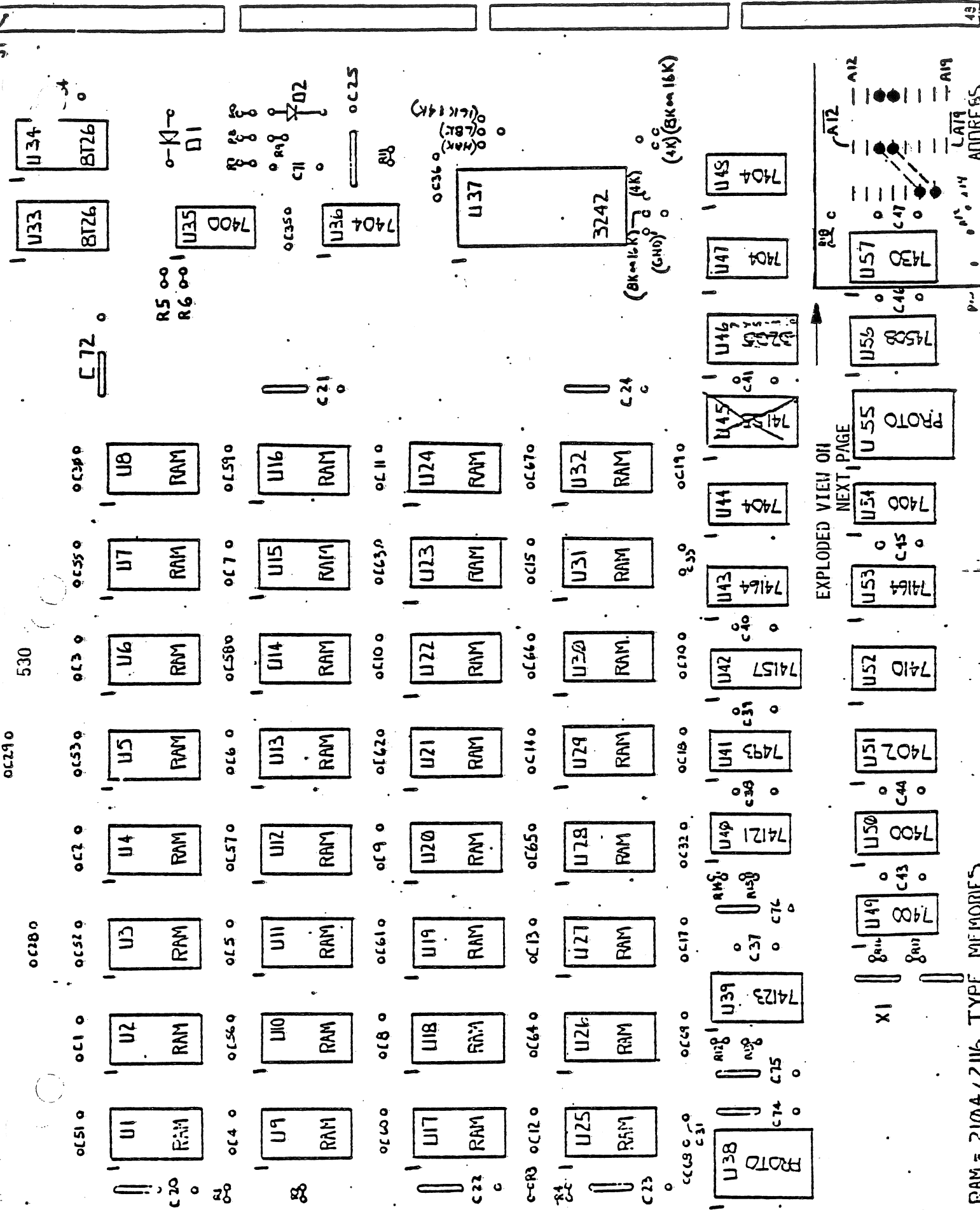
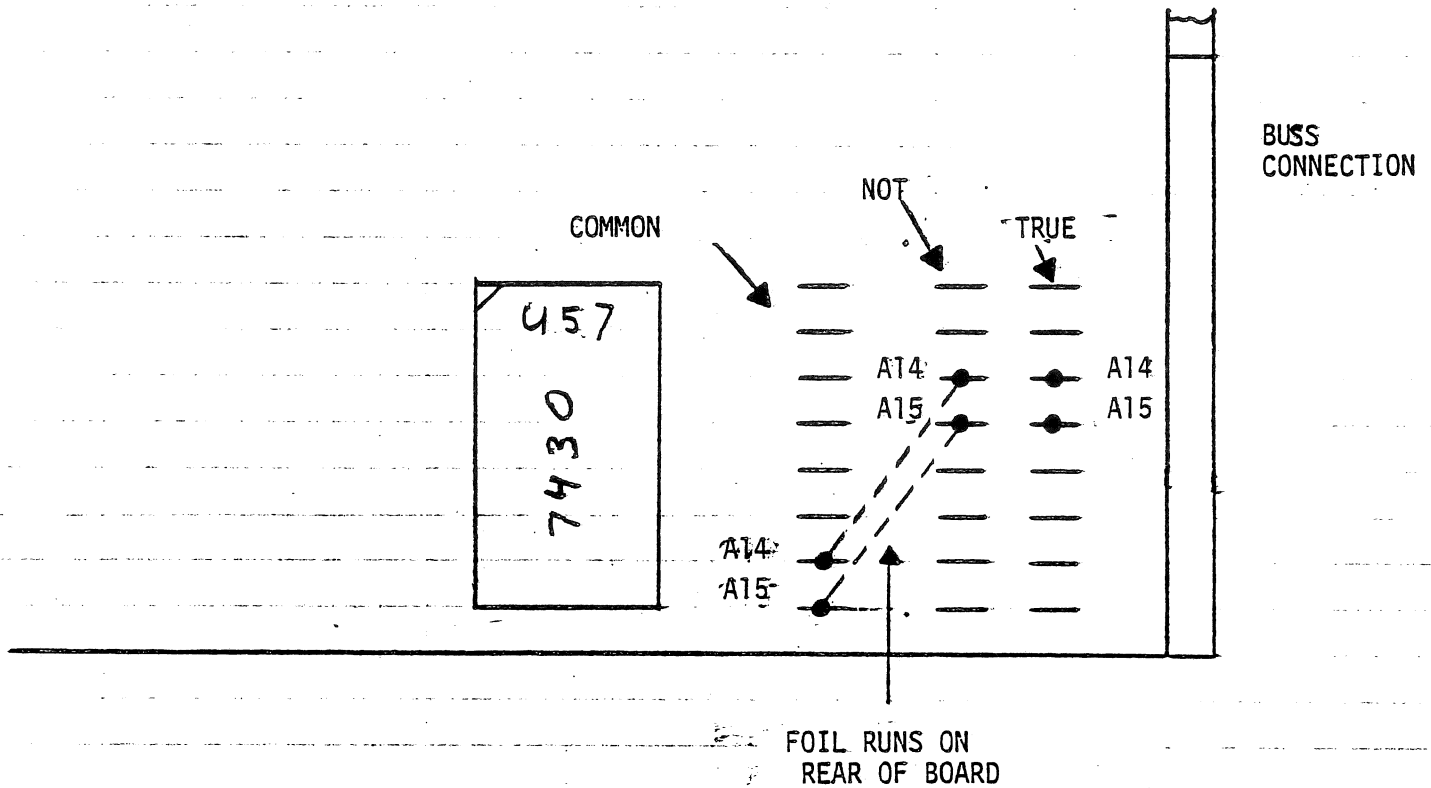THE CR MAY BE ELIMINATED BY THE FOLLOWING POKE:

POKE 2676,0

FOR EXAMPLE:

```
10   POKE 2683,0: POKE 2676,0:  REM KILL LF/CR
20   INPUT "TEST"; QA$
30   POKE 2683,10: POKE 2676,13:  REM RESTORE LF/CR
```

U34 BT26

U33 BT26

U35 740D

U36 7404

U37 3242

U45 7404

U47 7404

U46 3205

U44 7404

U43 74164

U42 74157

U41 7493

U40 74121

U39 74123

U38 PROTO

U48 7404

U57 7430

U56 74508

U55 PROTO

U54 7400

U53 74164

U52 7410

U51 7402

U50 7400

U49 7400

U8 RAM U7 RAM U6 RAM U5 RAM U4 RAM U3 RAM U2 RAM U1 RAM

U16 RAM U15 RAM U14 RAM U13 RAM U12 RAM U11 RAM U10 RAM U9 RAM

U24 RAM U23 RAM U22 RAM U21 RAM U20 RAM U19 RAM U18 RAM U17 RAM

U32 RAM U31 RAM U30 RAM U29 RAM U28 RAM U27 RAM U26 RAM U25 RAM

C72

530

EXPLODED VIEW ON NEXT PAGE

ADDRESS

A12   A19

RAM = 2104/2116 TYPE MEMORIES

EXPLODED VIEW OF LOWER RIGHT CORNER ON 530 16K DYNAMIC
MEMORY BOARD

BUSS
CONNECTION

COMMON   NOT   TRUE

457

7430

A14   A14
A15   A15

A14
A15

FOIL RUNS ON
REAR OF BOARD

NOTE: CUT THE TWO FOIL RUNS BETWEEN A14 COMMON - A14 NOT AND A15 COMMON - A15
NOT LOCATED ON THE FOIL SIDE OF THE BOARD BEFORE STRAPPING THE BOARD.

JUMPER TABLE

	1st 16K	2nd 16K	3rd 16K
A14 COM	A14 NOT	A14 TRUE	A14 NOT
A15 COM	A15 NOT	A15 NOT	A15 TRUE

JUMPER A14 COMMON AND A15 COMMON TO NOT OR TRUE ROWS FOR DESIRED 16K SLOT

Model 530

16K Dynamic RAM

Description:

The Model 530 - 16K dynamic board uses 4K x 1 4027 dynamic memories. Refreshes occur during Ø1 of the microprocessor's clock cycle and, therefore, are invisible to the user. The Model 530 requires power from +12 volts, 5 volts and -9 volts supplies. This excludes use in the 500-1 and Challenger IIP without additional supplies. Also, it is recommended that the 530 board be used in conjunction with the Model 580 backplane as this provides greater noise immunity than the 480 backplane.

Applications:

Low cost main memory in medium to large scale computer systems (16K to 48K or more).

Specifications:

Mechanical: 8" x 10" G-10 Epoxy Double-Sided Plated Through Hole Board.

Electrical: Power Requirements:

-9 volts at 4.8ma
+5 volts at 600ma
+12 volts at 328ma active
+12 volts at 248ma standby

Operating Frequency:

Clock must be 1MHz or slower and Ø2 must be at least 480ns long. Also, Ø1 must be at least 480ns long.

Available only as fully assembled, fully burned in memory board configured for 16K x 8 address strapable for any 16K partition within a 256K memory space (18 address bits).

Installation of CM-4 16K Dynamic Boards in Challenger II
Systems with 500 Boards.

Systems using CM-4 16K dynamic boards must meet the following
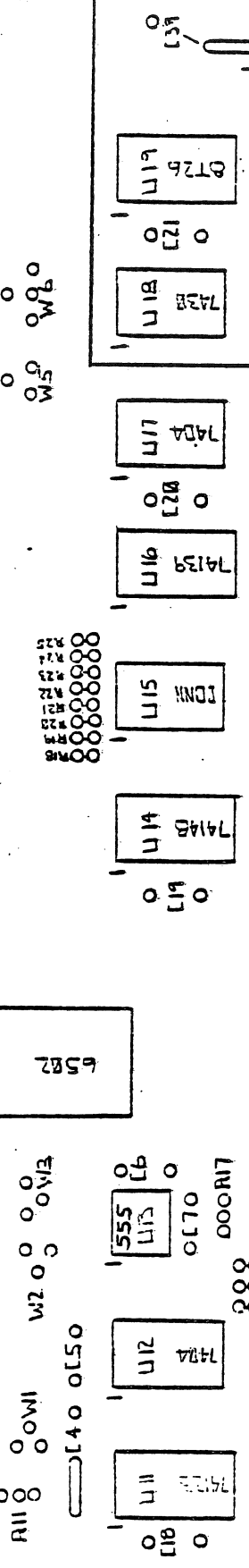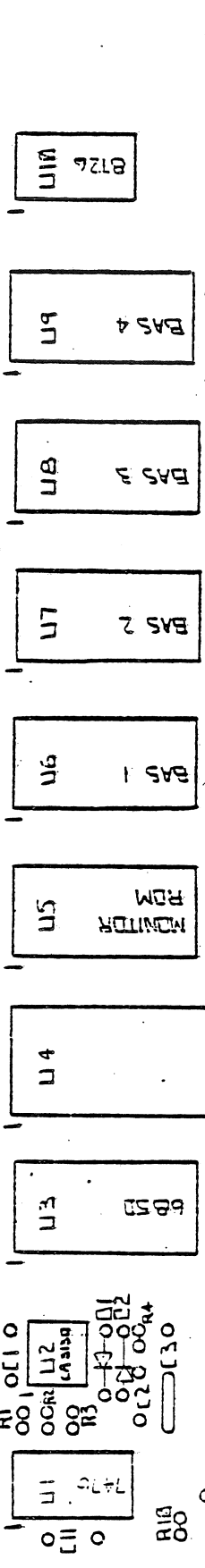specifications:

Clock must be 1 MHz or slower and Ø2 must be at least
480ns long.

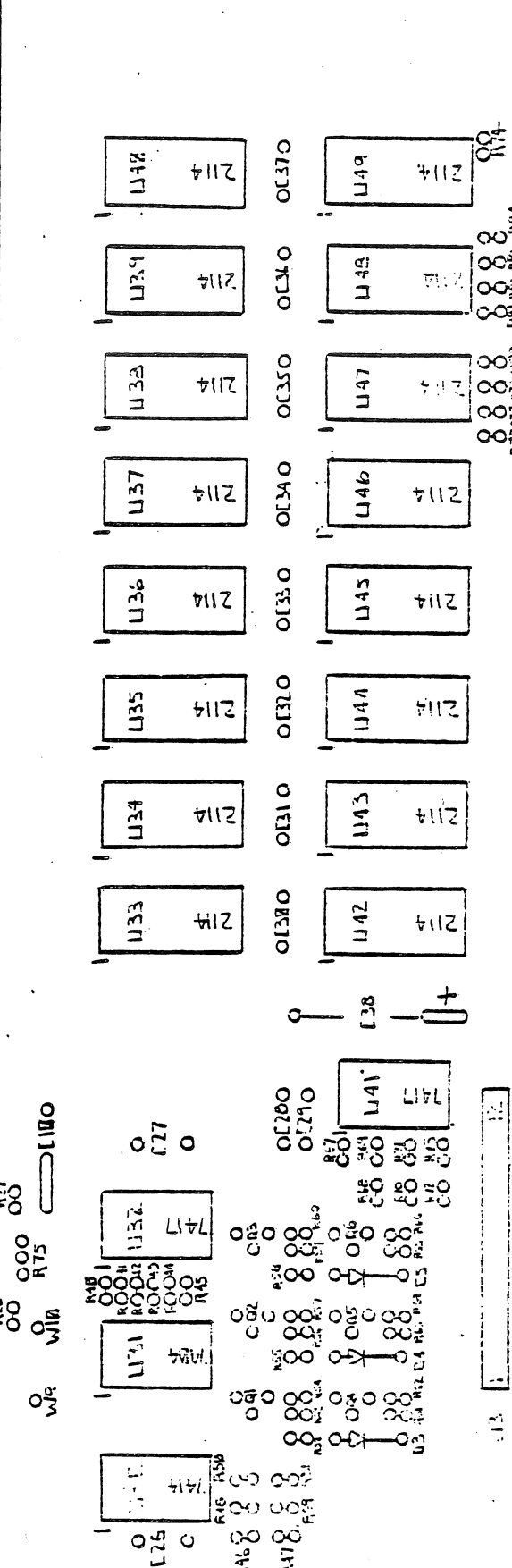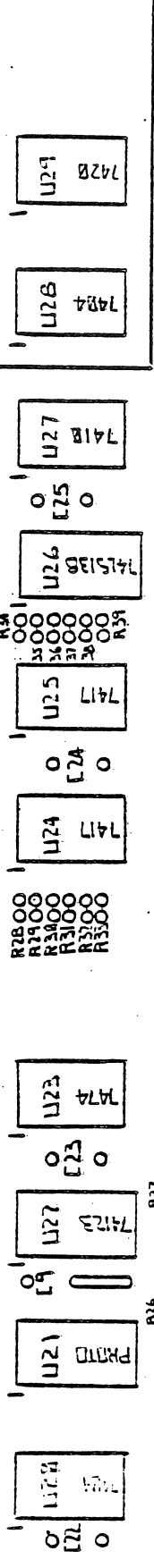Also, Ø1 must be at least 480ns long

To meet these specifications, 500 boards must be modified by
replacing capacitor C2 (82 pf.) with a 68 pf. capacitor and
readjusting the clock frequency for 950 KHz and checking that
Ø1 and Ø2 are at least 480ns long.

EXPLODED VIEW ON NEXT PAGE

U1 7417C
U2 LM339
U3 6821
U4 6582
U5 MONITOR ROM
U6 BAS 1
U7 BAS 2
U8 BAS 3
U9 BAS 4
U10 7417C
U11 7417B
U12 7418A
U13 7417B
U14 7414B
U15 LM324
U16 74134
U17 7404A
U18 7413B
U19 7417B
U20 7418A
U21 PHOTO
U22 7474
U23 7474
U24 741
U25 741
U26 74L513B
U27 7418
U28 7474
U29 7420
U31 PHOTO
U32 7417A
U33 2114
U34 2114
U35 2114
U36 2114
U37 2114
U38 2114
U39 2114
U40 2114
U41 741
U42 2114
U43 2114
U44 2114
U45 2114
U46 2114
U47 2114
U48 2114
U49 2114

555
W7
502

MEMORY STRAPPING FOR 502 CPU WITH 8K OF RAM

U18
7430

U19
8726

U7

A13 ———▶ ○   ○   ○ ◀——— A13
A14 ———▶ ○   ○   ○ ◀——— A14
A15 ———▶ ○   ○   ○ ◀——— A15

      ▲   ▲   ▲
   COMMON   NOT   TRUE

U28
7404

U29
7420

2ND BUSS
CONNECTOR

3RD BUSS
CONNECTOR
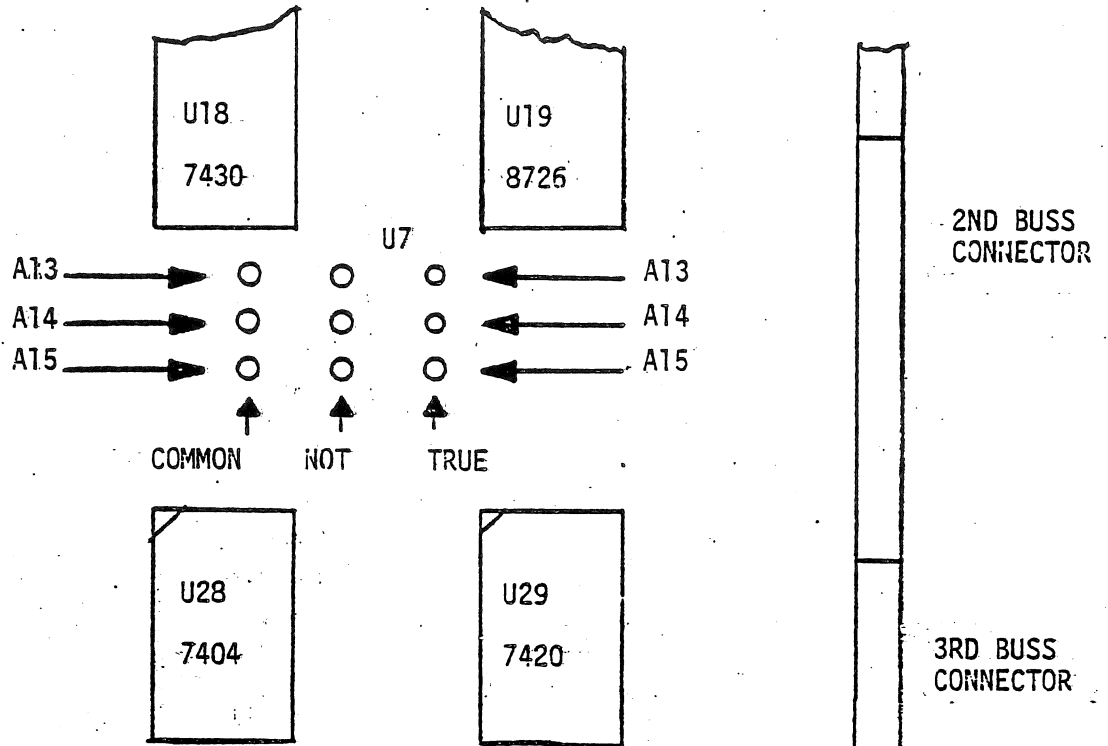
	1st 8K or 1st 4K	2nd 8K	3rd 8K	4th 8K
A13 COMMON	A13 NOT	A13 TRUE	A13 NOT	A13 TRUE
A14 COMMON	A14 NOT	A14 NOT	A14 TRUE	A14 TRUE
A15 COMMON	A15 NOT	A15 NOT	A15 NOT	A15 NOT
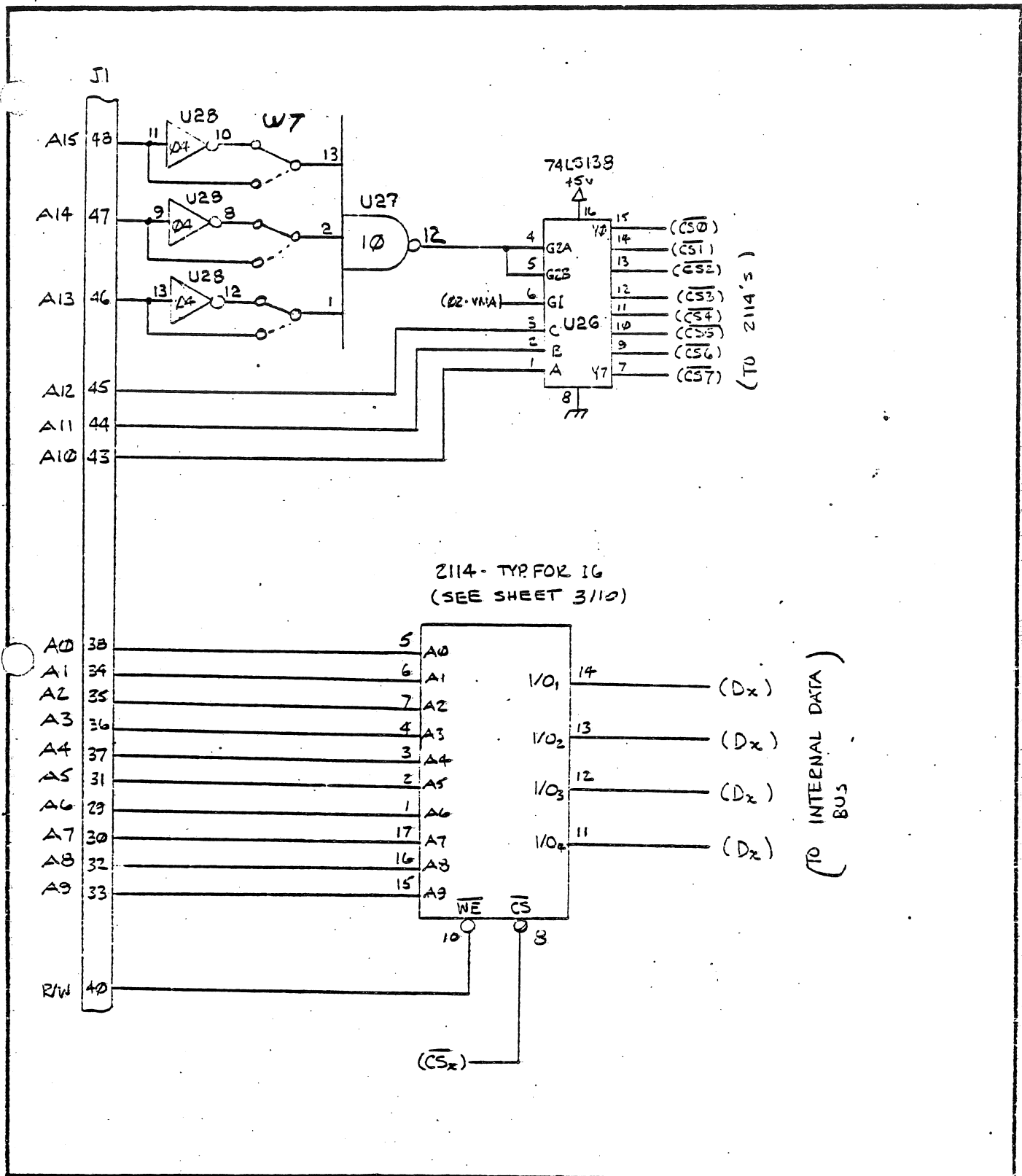
J1

A15 | 48   U28   W7
A14 | 47   U28   U27
A13 | 46   U28

74LS138

U26

(CS0)
(CS1)
(CS2)
(CS3)
(CS4)
(CS5)
(CS6)
(CS7)

(TO 2114's)

A12 | 45
A11 | 44
A10 | 43

2114 - TYP. FOR 16
(SEE SHEET 3/10)

A0 | 38   5   A0   I/O₁ 14   (Dx)
A1 | 34   6   A1
A2 | 35   7   A2   I/O₂ 13   (Dx)
A3 | 36   4   A3
A4 | 37   3   A4   I/O₃ 12   (Dx)
A5 | 31   2   A5
A6 | 29   1   A6   I/O₄ 11   (Dx)
A7 | 30   17 A7
A8 | 32   16 A8
A9 | 33   15 A9

(TO INTERNAL DATA BUS)

WE   CS
10   8

R/W | 40

(CSx)

OHIO SCIENTIFIC

ADDRESS SELECTION COMBINATIONS

WHEN USING THIS TABLE ONE MAY IGNORE THOSE ADDRESS LINES NOT PROVIDED ON THE MEMORY BOARD. FOR EXAMPLE: THE 520 16K STATIC RAM BOARDS PROVIDE JUMPER OPTIONS FOR A14 AND A15 ONLY. THEREFORE, IF ONE DESIRES, FOR EXAMPLE, TO STRAP THE BOARD FOR THE SECOND 16K SLOT ($4XXX) THE ONLY ADDRESS LINES TO CONCERN OURSELVES WITH ARE A14 AND A15. TO SET THE BOARD FOR $4XXX ONE WOULD JUMPER A14 COMMON TO A14 TRUE AND A15 COMMON WOULD BE JUMPERED TO A15 NOT (NORMALLY REFERRED TO AS NOT A15 OR /A15). A / BEFORE THE ADDRESS LINE E. G. /A12 READS AS A12 NOT OR NOT A12. IF THE ADDRESS LINE DOES NOT HAVE A / IN FRONT OF IT AND THE LINE IS NOT MARKED AS COMMON THEN THAT ADDRESS LINE IS TRUE, E. G. A12 IS THE SAME AS A12 TRUE.

ADDRESS	A12 COMMON TO	A13 COMMON TO	A14 COMMON TO	A15 COMMON TO
$0XXX	/A12	/A13	/A14	/A15
$1XXX	A12	/A13	/A14	/A15
$2XXX	/A12	A13	/A14	/A15
$3XXX	A12	A13	/A14	/A15
$4XXX	/A12	/A13	A14	/A15
$5XXX	A12	/A13	A14	/A15
$6XXX	/A12	A13	A14	/A15
$7XXX	A12	A13	A14	/A15
$8XXX	/A12	/A13	/A14	A15
$9XXX	A12	/A13	/A14	A15
$AXXX	/A12	A13	/A14	A15
$BXXX	A12	A13	/A14	A15
$CXXX	/A12	/A13	A14	A15
$DXXX	A12	/A13	A14	A15
$EXXX	/A12	A13	A14	A15
$FXXX	A12	A13	A14	A15