OHIO SCIENTIFIC TECH NEWS LETTER NUMBER TWO

It has come to our attention that many of you are not aware of the changes to the 510 CPU Board. We are currently shipping revision C of the 510 Board. The main difference between revision C and Revision B is the fact the 1702 support Eproms have been replaced by one support masked ROM (2316). This normally has no effect on the system with but two exceptions. The first exception is with respect to the CD-74 Hard Disc. Formally a 65H Hard Disc-Bootstrap Eprom was a required addition to any system desiring to boot directly from the hard disc. Now due to the masked ROM, the CD-74 Bootstrap routine is already on the board and is ready to go. However, the same bootstrap routine will not work for the CD-23. Therefore, one must replace the support ROM on the REV C Board with a SHMON 2758 Eprom. The revision B 510 Board requires the 65H-23 1702 Hard Disc bootstrap Eprom when used with the CD-23 Hard Disc. When placing orders for CD-23 Hard Discs, please include information specifying what revision of the 510 Board the CD-23 is to be used with. The table below outlines the different system configurations:

510 Revision B:

W/ CD-23 Requires 65H-23 1702 Disc Bootstrap Eprom
W/ CD-74 Requires 65H 1702 Disc Bootstrap Eprom

510 Revision C:

W/ CD-23 Requires SHMON 2753 support Eprom & Board changes
W/ CD-74 Requires no Board modification or extra parts

The Board modifications for the Rev C CD-23 are shown in the enclosed Schematic.

Creating 'Data File(s) Only' Diskettes Under OS-65U

OS-65U has two requirements for any diskette intended to be a 'Data File(s) Only' Diskette. The requirements are:

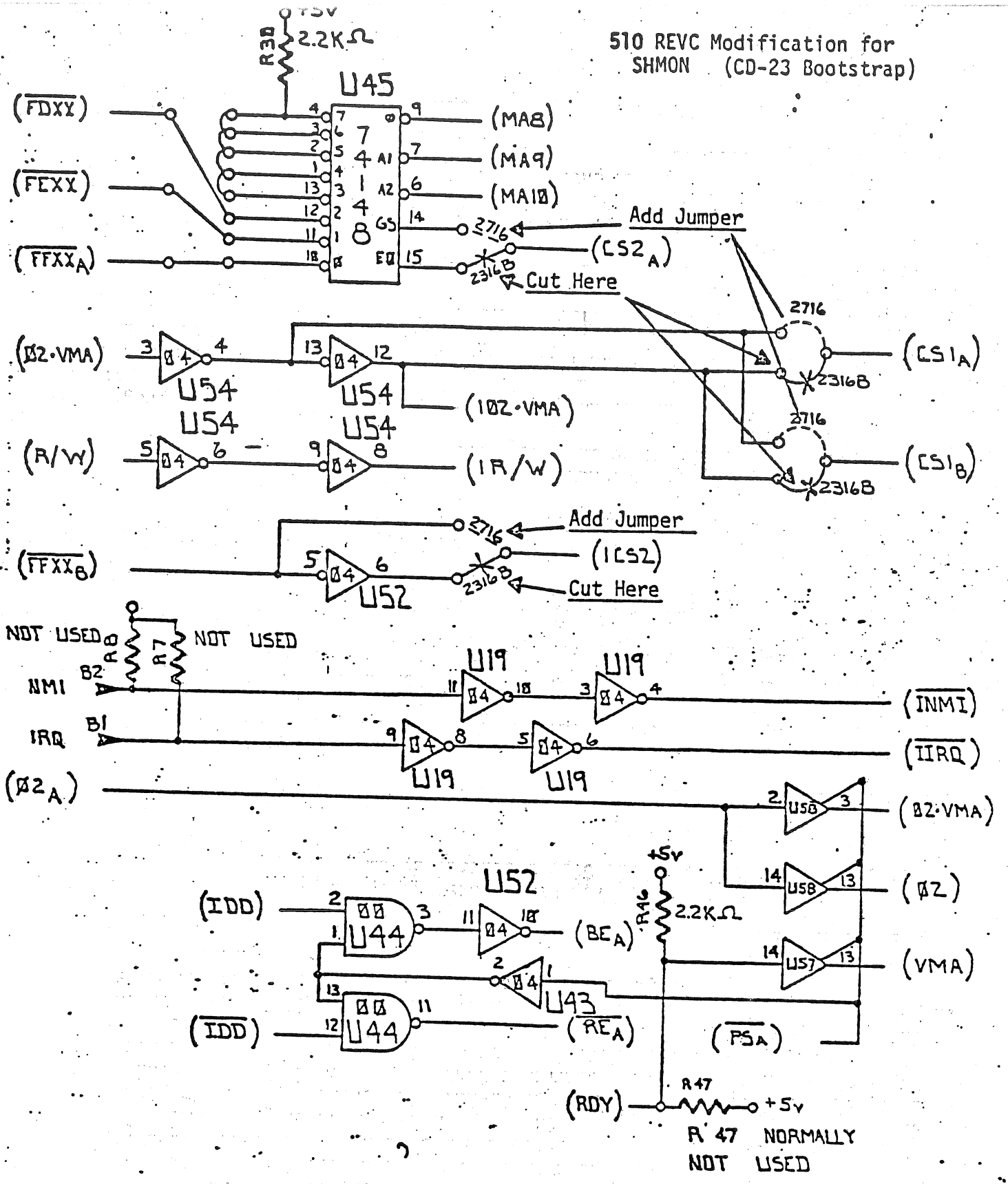
1) System must reside on diskette
2) First entry in directory must be 'DIREC*'

The System must reside on the diskette due to the fact that the copier program calls a page of code from the system portion of the diskette it is copying from. The reason that DIREC* must be the first entry is that this entry defines the location and size of the directory. The proper steps for the creation of a 'Data File(s) Only' Diskette are listed below:

1) Run 'Copier' and initialize the 'Data File(s) Only' Diskette from 0 to 275967
2) Copy the System portion of OS-65U to the 'Data File(s) Only' Diskette
3) Using 'Create' create an entry on the 'Data File(s) Only' Diskette as follows:

   A) File Name = DIREC*

510 REVC Modification for SHMON (CD-23 Bootstrap)



OHIO SCIENTIFIC			product name/number MODEL 510 REV C	
date 24 APR 1979	revision	page	status	sheet 2 of 11
DRAWN ~ J.L.K.				

B) Files Length = 1000
C) File Type = OTHER (O)
D) Access Rights = NONE (N)
E) Password = PASS.
F) After creation of the file is complete, Exit the Create Program (X) and type a Close CR.

The diskette may now be used as a 'Data File(s) Only' Diskette.

The following list contains a few memory locations and 'Pokes' of interest in OS-65U V1. 1.

Location of Control S, Q, C, O, D and W in OS-65U

Control Code	Contents	Run Time Address
Control S	19 ($13)	16086 ($3ED6)
Control Q	17 ($11)	16096 ($3EE0)
Control C	03 ($03)	16127 ($3EFF)
Control O	15 ($0F)	16131 ($3F03)
Control D	07 ($07)	16137 ($3F09)
Control W	23 ($17)	16139 ($3F0B)

*** POKES ***

This POKE permits one to respond with CR only in response to an input statement. String inputs return in null string and numberic inputs return the variable equal Zero.

```
POKE 2888, 0:  REM Normally (27)

POKE to permit , and : in input statements

POKE 2972, 13:  REM Permit ,  /  Normally (58)
POKE 2976, 13:  REM Permit :  /  Normally (44)
```

520 RAM Board with Respect to Level III

There are two corrections to the 520 Board required for its use in a Level III System. The first correction clears up noise problems on the 02*VMA Line during D1 of the System Clock. The correction should be made to all 520 RAMS Boards except those in the base partition (Partition F). The correction re-routes 02*VMA on its way to IC-O. 02*VMA is modified to first go through IC-I. Pin 6 of IC-I then is fed to pins 2 and 4 of IC-I. Note that the addition of the 68 PF Cap forms a RC noise trap via R4 and the 68 PF Cap. The second correction is a correction to the original 520 Board documentation. The memory management lines

A16 and A17 were shown reversed. The enclosed Schematic has been corrected.

Once again, we have found ourselves in a position of issuing a fix for a fix (as does anyone who issues corrections).. This fix is in reference to the Tech News Letter Number One. In particular, this fix references the patch for the undefined user function bug. The change is simply:

The original line read as:

000012DB 9B ? D4

The corrected line should read:

000012DB 9B ? D0

Use of 520 Memory Board in Level III Systems

To use 520 memory boards in Level III systems two changes re required. One is to address the memory boards for each partition and the other is to perform modifications to all 520 memory boards, except those at Partition F, to eliminate possible noise problems on the 02-VMA line during 01.

First, we will cover the addressing for multiple partitions. As 520 memory boards have only two additional addresses, A16 and A17, only four partitions may exist in a Level III system using 520 boards. Figure 35 contains the address jumpering information. Partition F will be where the main operating system resides with Partitions C, D and E being used for multiple users.

When using 520 memory boards in Level III systems, the following changes should be performed on all 520 boards except those at Partition F. The 520 boards at Partition F should be placed as close to the 510 board as possible. The recommended order in C3-B systems is as follows:

470	Floppy Interface
510	CPU
525	Dual Port
590	Hard Disk Controller
520	Memory Board
520	Memory Board
520	Memory Board

The remaining 520 memory boards should be placed in the front eight slots of the computer.

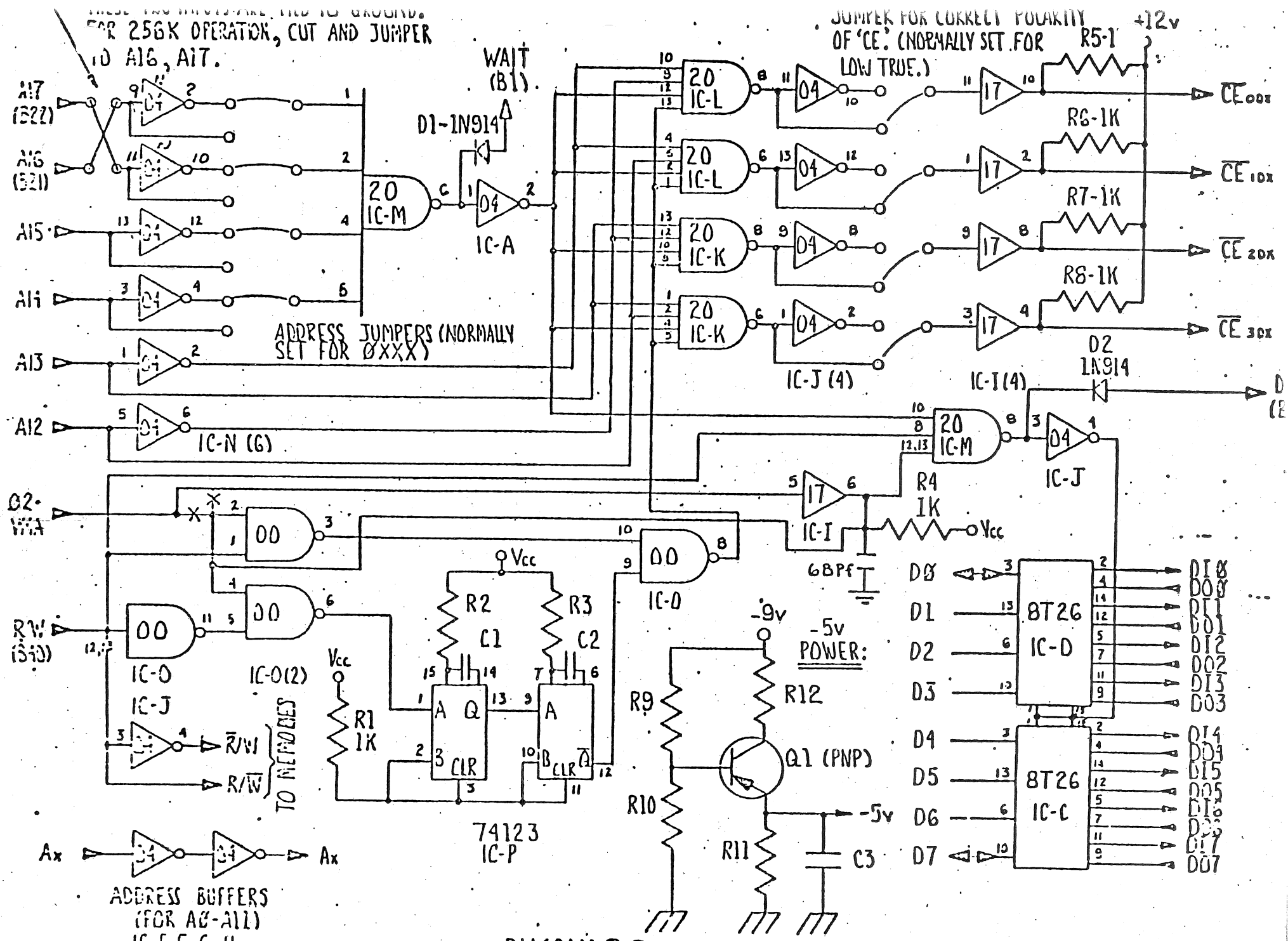
By placing the Partition F 520 memory boards in this order, and making the following modifications to the other 520 memory boards in the system, possible noise problems will be eliminated. Partition F is not modified so that triple processor capability is not affected. Refer to Figures 33 and 34 for sections of boards affected.

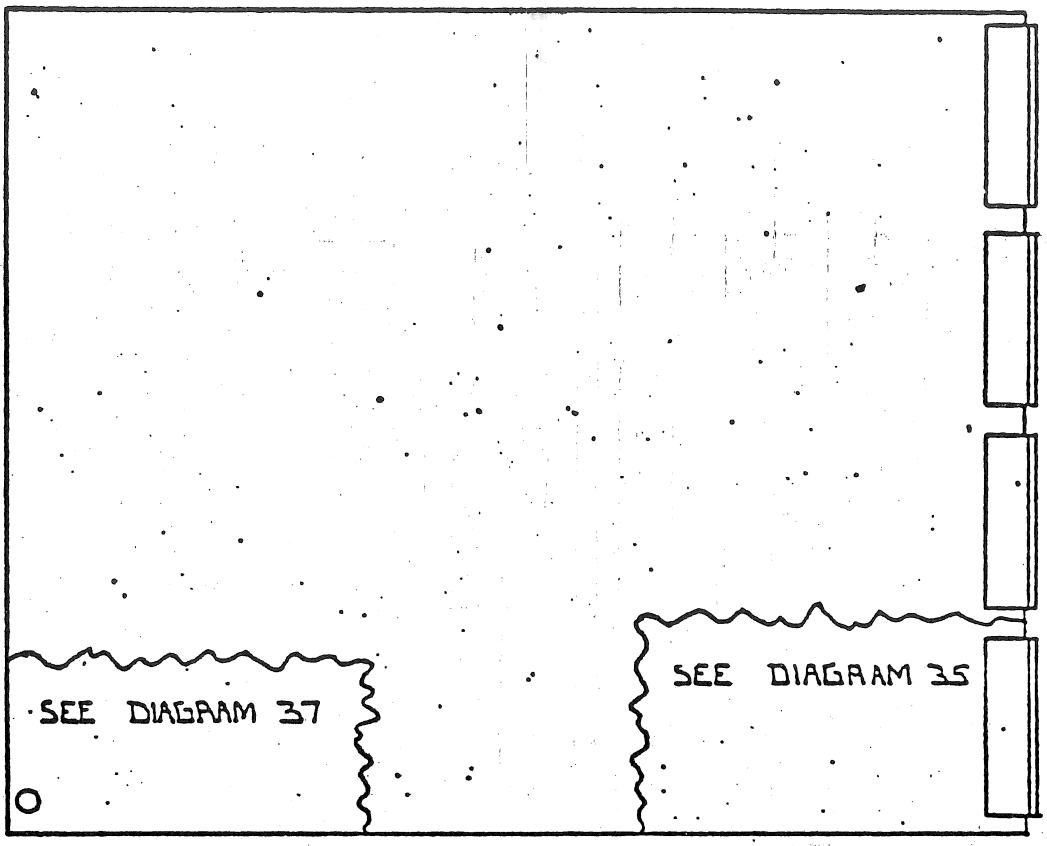
I. Cut the tape running from Pin 5 of IC-I (7417) going to Pins 2 and 4 of IC-0 (7400) as shown in Figure 36.

II. Jumper the tape that goes to Pins 2 and 4 of IC-0 (7400) to Pin 6 of IC-I (7417) as shown in Figure 36.

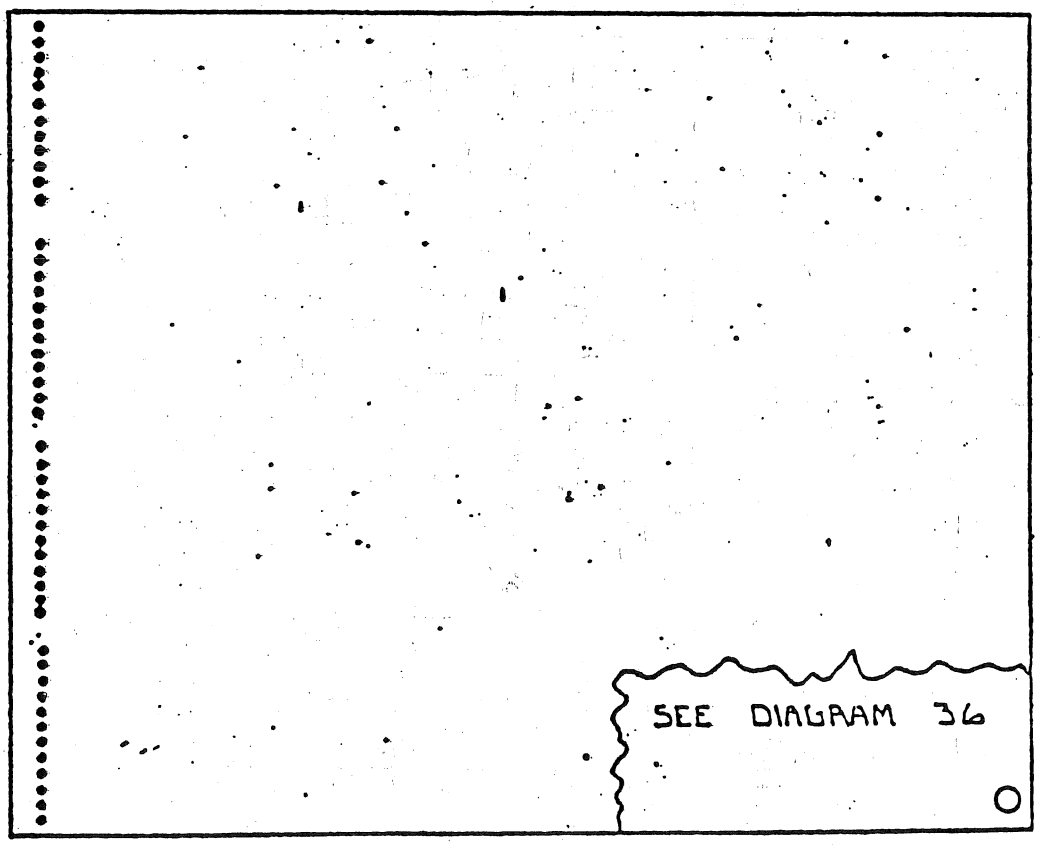
III. Install a 68 pf capacitor on the top side of the board from R4 (1K ohm resistor) on the side connected to Pin 6 of IC-I to ground as shown in Figure 37.

This completes the modifications to the 520 memory boards.


FOR 256K OPERATION, CUT AND JUMPER TO A16, A17.
JUMPER FOR CORRECT POLARITY OF 'CE.' (NORMALLY SET FOR LOW TRUE.)
+12v
R5-1K
R6-1K
R7-1K
R8-1K
WAIT (B1)
D1-IN914
D2 IN914
ADDRESS JUMPERS (NORMALLY SET FOR ØXXX)
IC-A
IC-J (4)
IC-I (4)
IC-N (G)
IC-M
IC-J
IC-I
R4 1K
Vcc
68Pf
IC-O
IC-O(2)
R1 1K
R2
R3
C1
C2
74123 IC-P
-9v
-5v POWER:
R9
R10
R11
R12
Q1 (PNP)
C3
8T26 IC-D
8T26 IC-C
TO REMODES
ADDRESS BUFFERS (FOR A0-A11) IC-E,F,G,H
DIAGRAM 38

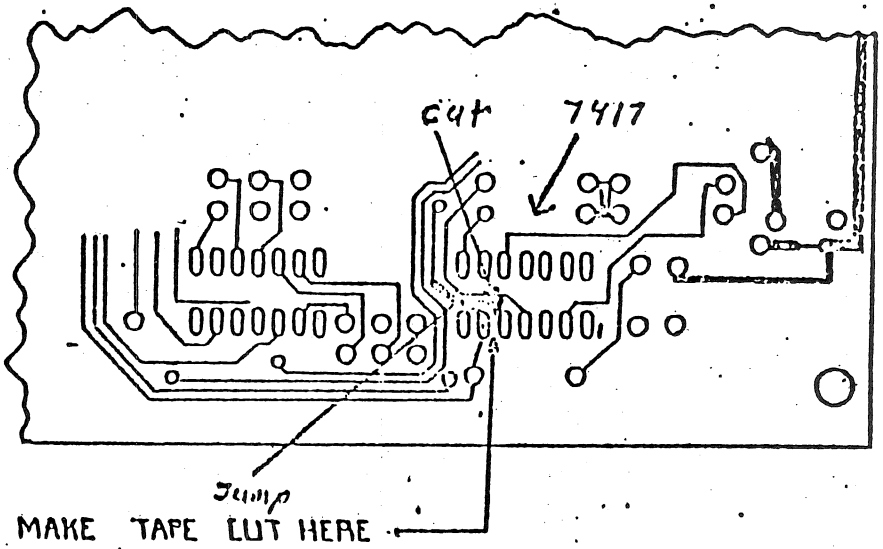


FRONT OF 520 BOARD
DIAGRAM 33



REAR OF 520 BOARD
DIAGRAM 34

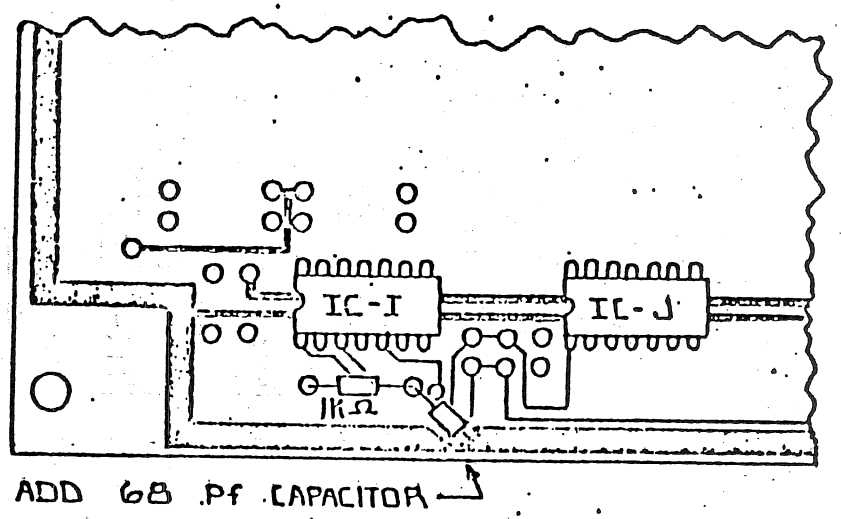
Cut foil run coming from pin 5 as shown. Then jumper pin 6 to foil run just cut from pin. 5.



MAKE TAPE CUT HERE AND JUMPER AS SHOWN.

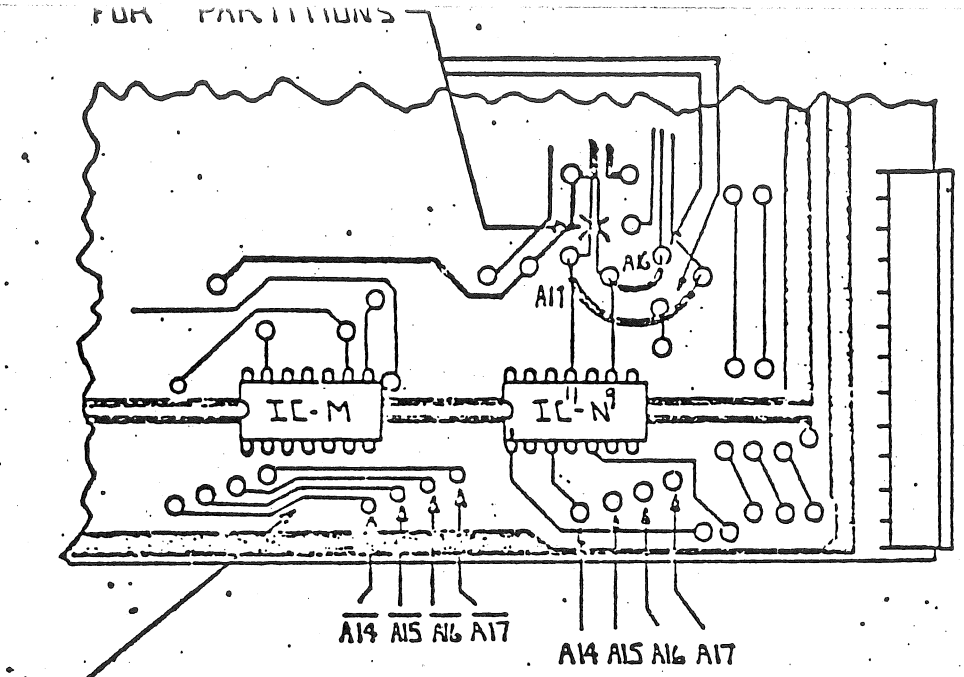
MODIFICATION TO REAR OF 520 BOARD FOR USE IN LEVEL III SYSTEMS

DIAGRAM 36



MODIFICATION TO FRONT OF 520 BOARD
FOR USE IN LEVEL III SYSTEMS

DIAGRAM 37



TO RE-ADDRESS BOARD,
CUT FOILS HERE AND
JUMPER NEW ADDRESS

DIAGRAM 35

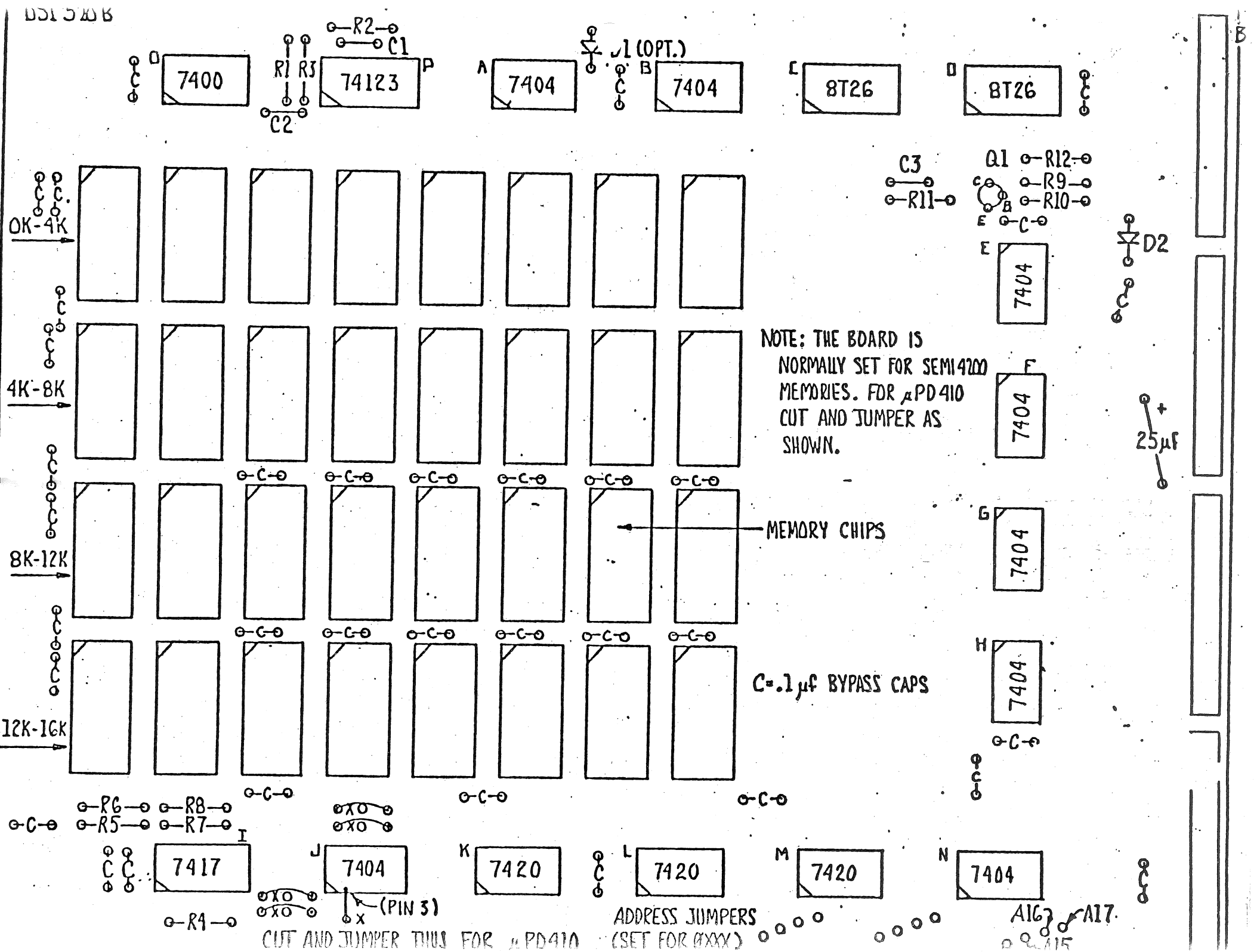
ADDRESS	BIT CONFIGURATION			
0XXX - 3XXX	$\overline{A14}$	$\overline{A15}$	X	X
4XXX - 7XXX	A14	$\overline{A15}$	X	X
8XXX - BXXX	$\overline{A14}$	A15	X	X
CXXX - FXXX	A14	A15	X	X

PARTITION				
C	X	X	$\overline{A16}$	$\overline{A17}$
D	X	X	$\overline{A16}$	A17
E	X	X	A16	$\overline{A17}$
F	X	X	A16	A17

X = IRRELEVANT

MODEL 520 IS NORMALLY SET FOR PARTITION C,
ADDRESS 0XXX - 3XXX.
FOR OTHER LOCATIONS, CUT AND JUMPER AS DESIRED.

MODEL 520 - ADDRESS JUMPER INFORMATION


7400
R1
R3
R2
C1
C2
74123
A
7404
J1 (OPT.)
B
7404
E
8T26
D
8T26
C3
R11
Q1
R12
R9
R10
E
7404
D2
NOTE: THE BOARD IS NORMALLY SET FOR SEMI 9200 MEMORIES. FOR μPD410 CUT AND JUMPER AS SHOWN.
F
7404
25μf
0K-4K
4K-8K
8K-12K
12K-16K
MEMORY CHIPS
G
7404
H
7404
C=.1μf BYPASS CAPS
R6
R5
R8
R7
I
7417
J
7404
(PIN 3)
K
7420
L
7420
M
7420
N
7404
R4
CUT AND JUMPER THUS FOR μPD410
ADDRESS JUMPERS (SET FOR 0XXX)
A16
A17
A15